MULTI-REGIONAL CHARGE-BASED SMALL-SIGNAL BIPOLAR JUNCTION TRANSISTOR MODEL

By

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Abstract of Dissertation Presented to the Graduate School of the University of Florida in Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy

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In this dissertation, a multi-regional charge-based small-signal bipolar junction transistor (BJT) model based on the one-dimensional charge-based model is presented. Such a model is necessary for the device and circuit simulation of advanced high speed BJTs. The multi-regional charge-based BJT model is composed of models for the intrinsic transistor, the peripheral (side-wall) transistor, the intrinsic base resistance, and the extrinsic p+/n diode. A charge-based bipolar transistor which has been developed by H. Jeong and J. G. Fossum is used as the basis for this scalable transistor model. A physical intrinsic base resistance model is developed in conjunction with the charges and currents defined by the one-dimensional model and includes the emitter crowding , high-injection in the base, and base push-out. A

technique for the separation of the emitter-base and base-collector junction capacitances among the intrinsic, peripheral, and extrinsic region is developed and verified with measurement The collector and base currents are separated between the intrinsic and peripheral transistors by measuring transistors of varying emitter area. Using this approach, the charges and currents of the peripheral transistor are proportional to that of the intrinsic transistor by the ratio of their emitter periphery to area and by an empirical proportionality constant. The resulting multi-regional charge-based large-signal BJT model is implemented into SLICE using user-defined controlled sources and verified for dc measurement on transistors of varying emitter area. The multi-regional small-signal charge-based BJT model is derived from this scalable large-signal model. The s-parameter measurement and calibration technique are explained. These ac data (s-parameter measurement) are compared with simulated data for the small-signal model. Preliminary small-signal model verification is achieved for the (common-emitter) base input port, but it is concluded that the verification of the collector output port awaits better data acquisition techniques.

CHAPTER 1
INTRODUCTION

To improve the frequency response and the switching speed of bipolar transistor, the transistor has been scaled down using a double-polysilicon, self-aligned structure [ZDEB87] and, concomitantly, packing densities have increased substantially. The polysilicon emitter contact layer is doped by ion implantation and serves as a dopant source for the underlying emitter. This polysilicon contact process reduces base current (keeps current gain high) and makes vertical scale down possible. The polysilicon base contact process also allows for reduction in the base resistance and the base-collector junction capacitance. Both of the improvements result in improved device speed. As a result, the self-aligned polysilicon contact BJT performance is greatly improved.

Improved models for these advanced bipolar transistors which include the multi-dimensional nature and high-current effects in both the base and collector need to be incorporated into the computer simulation tools such as SPICE2. The ratio of peripheral (side-wall) transistor collector current to intrinsic region collector current

increases in advanced BJTs as the emitter area becomes smaller [REIN87] and the transistors are operated at higher current densities for speed improvement. Unfortunately, the Gummel-Poon model used in SPICE is a one-dimensional empirical model and cannot be used to simulate advanced-structure BJTs accurately. A more accurate scalable BJT model is demanded for reliable circuit simulation.

A very physical one-dimensional charge-based BJT model has been developed by H. Jeong and J. G. Fossum [JEON89] which may replace the conventional Gummel-Poon model in SPICE. The model has in it a complete model for high current effects in the collector as well as the base. This model solves the regional transport and the moving boundary conditions by an (semi-numerical) iterative process of matching an collector current calculated in collector region with that in the base region derived from a knowledge of the doping profile in the base and collector, the junction depth and the layout information.

While this model is an improvement over the Gummel-Poon model, it does not include the extrinsic multi-dimensional effects of advanced BJTs and a model for the intrinsic base resistance which is critical to accurate simulation of frequency response. Many papers about two-dimensional effects have been published [REIN84, REIN87, HURK87]. For two-

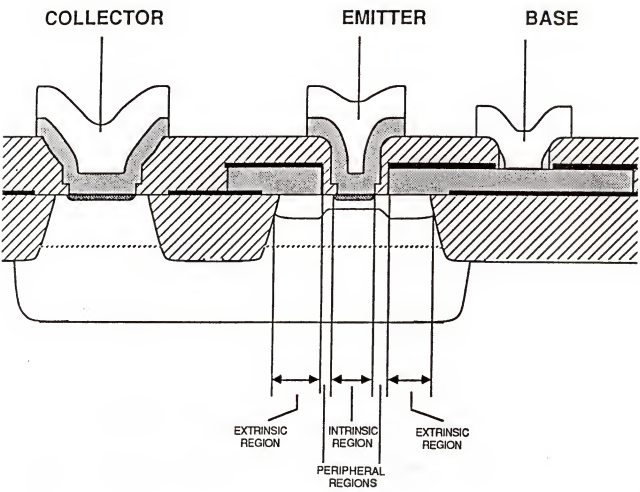


Fig. 1.1 Cross-sectional view of a self-aligned double-polysilicon BJT. The transistor is divided into three regions: intrinsic region, peripheral region, and extrinsic region. A typical transistor will have an emitter window area of 1.5 X 4 μm^2, an emitter junction depth of ~.1 μm.

dimensional small-signal analysis, the intrinsic base resistance [HAUS64, VALS86, LAUX85, LUO87], the peripheral (side-wall) region transistor, and the extrinsic collector-base diode region are important (see Fig. 1.1). Each of these regions has to be incorporated separately into the BJT model for high speed (> 1 GHz) operation.

The objective of this dissertation is to develop a multi-regional small-signal BJT model. The multi-regional small-signal model is derived from a multi-regional large-signal model. For this purpose, a one-dimensional charge-based large-signal model developed by H. Jeong and J. G.Fossum [JEON89] is adopted. As pointed out above, this model is used not only because it is more physical than the empirical Gummel-Poon model, but also because it includes a physical representation of high-current effects.

The main tasks presented in this dissertation are as follows:

(1) developing a physical model for the intrinsic base resistance in low- and high- current operation,

(2) development of a new technique to separate the junction capacitances among the intrinsic, the peripheral and the extrinsic regions,

(3) derivation of multi-regional charge-based small-signal model from a multi-regional charge-based large-signal model,

(4) implementation of the developed multi-regional charge-based large-signal model into SLICE [HARR84] using user-defined controlled sources and development small-signal circuit simulator (SMACS) for small-signal model simulation,

(5) verification of the multi-regional large and small-signal model using dc and ac (s-parameter) measurement, respectively, and

(6) introduction of s-parameter measurement and calibration technique.

In Chapter 2, the one-dimensional charge-based BJT model [JEON89] is reviewed because it is the basis for the intrinsic and peripheral transistor models in the multi-regional charge-based BJT model. The base and collector analysis and the linkages between these regions is described, and the network representation is also shown.

In Chapter 3, the physical model for the intrinsic base resistance is described. It is adapted from Hauser's base resistance model [HAUS64] which includes emitter crowding effect. This model is extended to include high current effects such as the base push-out and high-level injection in

the base and collector. The intrinsic base resistance model is linked with one-dimensional intrinsic charge-based transistor model which supplies physical parameters as a function of bias to intrinsic base resistance model. The resulting model is valid at low-current and high-current regions; it is physical and no extra model input parameters are needed.

In Chapter 4, a method for the separation of junction capacitance is developed. To accurately model the multi-regional transistor model, it is necessary to separate junction capacitances into intrinsic and peripheral region capacitances. Using the measured capacitance data of different emitter size transistors, and a non-linear least square fitting method, junction capacitances are successfully separated. This technique does not require any calibration procedure to subtract out the effect of the parasitic capacitances.

In Chapter 5, the complete multi-regional charge-based large-signal model is described from the modeling explained in previous chapters. This model is implemented in SLICE [HARR88] using user-defined controlled sources. The multi-regional charge-based small-signal model is derived from this multi-regional charge-based large-signal model. Because transcapacitance elements are not available in SPICE2, a

small-signal circuit simulator (SMACS) has been developed to simulate this multi-regional small-signal model.

In Chapter 6, the dc measurements are compared with the multi-rigional large-signal model simulation using user-defined controlled sources (UDCSs) [HARR84] for dc verification. For ac verification, the ac (s-parameter) measurements are compared with SMACS simulation results. Since the test transistor's cut-off frequencies are above 1 GHz, the network analyzer is used to measure the s-parameter. The s-parameter measurement and calibration techniques are also discussed.

In Chapter 7, the conclusions are drawn and future work is outlined.

CHAPTER 2
ONE-DIMENSIONAL CHARGE-BASED BIPOLAR TRANSISTOR MODEL

2.1 Introduction

As explained in Chapter 1, the multi-regional charge-based BJT model is composed of three regions. For intrinsic transistor, the one-dimensional charge-based large-signal model developed by H. Jeong and J. G. Fossum [JEON89] is used.

This model is quite different from the Gummel-Poon model. The latter is a empirical, analytical and charge-control model, whereas the former is a physical, semi-numerical and charge-based model. It requires approximately 30 parameters most of which can be taken from transistor layout and profile information.

In the one-dimensional charge-based model, the high-current effects are modeled in the collector region (Section 2.2). The carrier transport problem in the quasi-neutral base (QNB) region for an exponential doping profile is solved analytically. The base- and collector-region analyses are linked through the base-collector boundary conditions. The base region analysis are described in Section 2.3. The physical linkages between the base and collector transports

and the network representation of the one-dimensional charge-based model are described in Section 2.4.

2.2 Collector Analysis

A quasi-saturation model for the collector has been developed by Kull [KULL85]. H. Jeong and J. G. Fossum extended this model to include the formation of a current-induced space-charge region (SCR) at sufficiently high currents [JEON87]. As shown by the numerical simulations of the base push-out [ZDEB87], for advanced BJT, the formation of the SCR significantly affects the high-current characteristics. In the charge-based BJT model, the carrier transport in the SCR of the collector is analyzed, and the analysis is coupled through boundary with that for the adjacent quasi-neutral-region (QNR) of the collector to yield an implicit characterization of the collector current, I_C (V_{BCO}, V_{BC}), in terms of the base-collector voltage and the quasi-Fermi potential separation V_{BCO} at the base-collector junction. This characterization is combined with the base transport analysis to completely define the current-voltage characteristics of the transistor. The stored charges Q_{SCR} and Q_{QNR} in the SCR and QNR ,respectively, of the collector are implicitly characterized based on the transport analysis.

Because I_C can be greater than I_O, the saturated drift-velocity current in the unmodulated epitaxial collector qAv_sN_{EPI}, in the saturation region ($V_{BC} > 0$) without forming the current-induced SCR, the maximum possible collector current compatible with the quasi-neutrality at $x = x_{HL}$ (see Fig. 2.1) is specified as

$$I_{SCR} = qAv_s n(x_{HL}) \tag{2.1}$$

where

$$n(x_{HL}) = \frac{N_{EPI}}{2}\left\{1 + \sqrt{1+\left(\frac{2n_i}{N_{EPI}}\right)^2 \exp\left(\frac{V_{BC}}{V_T}\right)}\right\} \tag{2.2}$$

is defined by the pn product and the quasi-neutral condition at x_{HL}. The quasi-neutral condition is used for evaluating V_{BCI}, the quasi-Fermi potential separation at the surface (x_I) between the SCR and the QNR:

$$V_{BCI} = V_T \ln\left[\frac{I_C(I_C - I_O)}{(qAv_s n_i)^2}\right]. \tag{2.3}$$

This ensures the continuity of the current characterization at $I_C = I_{SCR}$.

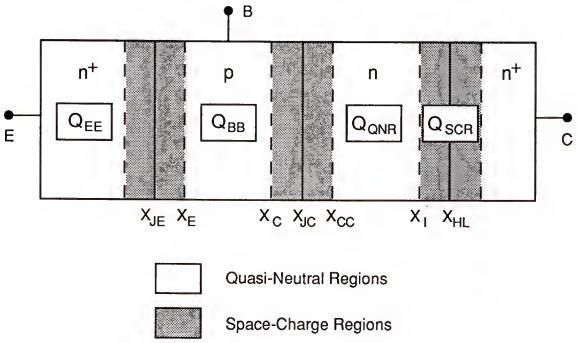


Fig. 2.1 One-dimensional structure of an n^+-p-n-n^+ epitaxial bipolar transistor with its regional boundaries labeled and regional charges indicated.

The junction space-charge region is included to account for the effect of the space-charge region at the base-collector junction and to facilitate proper connections among the different regions of operation. The extent or size of W_{SCC}, the SCR on the collector side, is the criteria for checking the operating conditions in the collector and provides a basis for collector analysis. It is assumed that the integral of the electric field across the entire epitaxial collector region equals the junction built-in potential ϕ_C plus the reverse-bias voltage V_{BC}. The W_{SCC} is expressed in terms of I_C by applying Poisson's equation to the junction space-charge region:

$$W_{SCC} = \sqrt{\frac{2\varepsilon A v_s \left(\phi_C - V_{BC} - I_C R_{EPI}\right)}{\left(I_O - I_C\right)}} \tag{2.4}$$

where $R_{EPI} = W_{EPI} / qA\mu_n N_{EPI}$.

Overviewing [JEON87] and extension involving (2.4), the possible conditions (refer to Fig. 2 in [JEON87]) in the epitaxial collector as controlled by V_{BE} and V_{BC} are as follows. If W_{SCC} equals 0, i.e., if

$$I_C \geq \min \left\{ I_O,\ I_{OOS} \equiv \frac{\phi_C - V_{BC}}{R_{EPI}} \right\} \equiv I_{SCC} \tag{2.5}$$

then, as [JEON87] characterizes, the collector comprises the QNR, adjacent to the base, and a possible current-induced SCR, which can cover the entire epitaxial collector. If (2.5) is not satisfied, then the junction space-charge region exists, which can also cover the entire epitaxial collector. For W_{SCC} greater than 0, the collector analysis simply defines the boundary conditions for the base analysis.

2.3 Base Analysis

De Graaff and Kloosterman [GRAA85] have solved carrier transport problem in the QNB for a representative exponential doping profile, and thereby have demonstrated the dependence of the base transit time on built-in electric field and bias conditions. However, they first assume a constant QNB width, and then as a function of bias perturb the solution of the QNB width to empirically derive the base-width modulation. This, in effect, unrealistically portrays the doping profile as being dependent on bias, because its expression depends on the arbitrary QNB width.

H. Jeong and J. G. Fossum have extended this model and have reduced the empiricism in the determination of the base-width modulation. They define the doping profile as in [GRAA85], but explicitly account for the moving boundaries of the QNB. Thus, it is assumed that

$$N_A(y) = N_{AO} \exp\left(-\frac{\eta y}{W_{BO}}\right) \tag{2.6}$$

where W_{BO} is the QNB width, N_{AO} is the peak doping density at the emitter side of QNB at equilibrium, and η is the exponential factor of QNB.

If the hole current is negligible, then the base transport current can be expressed as [GRAA85]

$$I_C = -qA\overline{D_n}\left(\frac{2n + N_A}{n + N_A}\frac{dn}{dy} + \frac{n}{n + N_A}\frac{dN_A}{dy}\right) \tag{2.7}$$

where n and N_A are electron density and doping density in QNB, respectively, and $\overline{D_n}$ is the average electron diffusivity in QNB.

Except for hard saturation, (2.7) is valid for all modes of operation. Integrating (2.7) over the QNB width W_B, from y_E to y_C (see Fig. 2.1), analytical solutions, I_{CL} and I_{CH}, for low and high injection are obtained, respectively,

$$I_{CL} = \frac{qA\overline{D_n}\eta}{W_{BM}}\left(\frac{fn_E - n_C}{f - 1}\right) \equiv I_{CLF} - I_{CLR} \tag{2.8}$$

$$I_{CH} = \frac{2qA\overline{D_n}\eta}{W_{BM}}\left(\frac{n_E - n_C}{\ln(f)}\right) \equiv I_{CHF} - I_{CHR} \tag{2.9}$$

where $n_E \equiv N_A(y_E)$, $n_C \equiv n(y_C)$, and $f \equiv \exp(\eta W_B/W_{BO})$. For ease

of interpolation for intermediate injection, I_{CL} and I_{CH} are decomposed into forward and reverse components as indicated in (2.8) and (2.9), respectively. The closed-form expression for the forward or reverse component of I_C, for all injection levels, is given by a weighted linear sum of the corresponding low- and high- injection solutions [GRAA85]:

$$I_C = I_{CF} - I_{CR} = \frac{I_{CLF} + C_F \frac{n_E}{N_{AE}} I_{CHF}}{1 + C_F \frac{n_E}{N_{AE}}} - \frac{I_{CLR} + C_R \frac{n_C}{N_{AC}} I_{CHR}}{1 + C_R \frac{n_C}{N_{AC}}} \tag{2.10}$$

where $N_{AE} \equiv N_A(y_E)$, $N_{AC} \equiv N_A(y_C)$, and C_F and C_R are coupling coefficients.

For the transient model, the stored charge in the base region is now considered. Q_{BB}, the total hole charge in the QNB, is evaluated from I_C in (2.10) by using the fundamental Moll-Ross relation [MOLL56]:

$$Q_{BB} \equiv qA \int_{x_E}^{x_C} p \, dx$$

$$= qA \frac{q A \overline{D_n} n_i^2}{I_C} \left[\exp\left(\frac{V_{BE}}{V_T}\right) - \exp\left(\frac{V'_{BCO}}{V_T}\right) \right] \tag{2.11}$$

where V'_{BCO} is the quasi-Fermi potential separation at $y = y_C$.

This characterization is not only physically sound, but it is computationally efficient and it eliminates the need for another interpolation for the charge as a function of bias as was done in [GRAA85]. Regions of operation where (2.10) and (2.11) are invalid such as in hard saturation, are narrow, and are accounted for by extrapolation.

2.4 Base and Collector Linkages and Network Representation

The solutions of transport in QNB are explicit functions of boundary locations (y_E and y_C) as well as carrier densities (n_E and n_C) at the boundaries.

The boundary conditions at $y = y_E$ can be defined straightforwardly via the emitter-base junction SCR analysis. On the other hand, the boundary conditions at $y = y_C$ are dependent on the collector transport, and hence link the base and collector transports.

The carrier density at $y = y_E$ is evaluated from the pn product by using quasi-neutrality:

$$n_E = \frac{N_{AE}}{2}\left[\sqrt{1 + \left(\frac{2n_i}{N_{AE}}\right)^2 \exp\left(\frac{V_{BE}}{V_T}\right)} - 1\right]. \qquad (2.12)$$

The boundary location y_E is the metallurgical junction location (y_{JE}) plus the width of the space charge region on

the base side of the emitter-base junction. This width is semi-physically modeled [LIOU87] as follows:

$$W_{SE} = W_{SEO}\left[\frac{\phi_E - V_{BE}}{\phi_E}\right]^{m_E} \quad \text{for } V_{BE} \le \phi_E - \Delta\phi_E \tag{2.13}$$

$$= W'_{SEO}\exp\left(-\frac{V_{BE}}{4V_T}\right) \quad \text{for } V_{BE} > \phi_E - \Delta\phi_E \tag{2.14}$$

where W_{SEO} is the base-emitter junction SCR width on the base-side at equilibrium, and W'_{SEO} and $\Delta\phi_E$ are related to W_{SEO} and m_E by imposing the continuities of W_{SE} and its derivative with respect to V_{BE} at $V_{BE} = \phi_E - \Delta\phi_E$.

The boundary conditions at $y = y_C$, which link the base and collector analysis, are established in a similar manner in terms of V_{BCO}; thus $n_C(V_{BCO})$ and $W_{SC}(V_{BCO})$ are described by equations analogous to (2.13) and (2.14). There are, however, notable exceptions to these boundary conditions when there is the current-induced SCR in the collector side of the base-collector junction. Thus, the magnitude of the electric field at the metallurgical juction, E_J, is adopted.

Applying Poisson's equation to the space-charged epitaxial collector and again noting the integral of the electric field over this region equals $\phi_C - V_{BC}$, E_J yields:

$$E_J = \frac{W_{EPI}\,(I_O - I_C)}{2\varepsilon A v_s} + \frac{\phi_C - V_{BC}}{W_{EPI}} \quad . \tag{2.15}$$

By neglecting the mobile carrier charges in the SCR on the base side of the base-collector junction, the SCR width on the base side is expressed as:

$$W_{SC} = \frac{W_{BO}}{\eta} \ln\left(\frac{E_J + E_O}{E_O}\right) \tag{2.16}$$

where $E_O = q\,N_A(y_{JC})\,W_{BO}/\varepsilon\eta$. Thus, $y_C = y_{JC} - W_{SC}$, and, in this case, $n_C = I_C/qAv_s$ is assumed to be limited by the electron velocity saturation.

Thus, the linkage between the base and collector analysis involves either V_{BCO} or E_J. The QNR disappears in the collector region because either the junction space-charge region (W_{SCC} -> W_{EPI}) or the current-induced SCR (W_{SCR} -> W_{EPI}) expands to cover the entire region. For the first case, $W_{SCC} = W_{EPI}$ which, with (2.4), defines the relations between V_{BC} (= V_{BCO} when $W_{QNR} = 0$) and I_C at the onset ($I_C = I_O$). For the second case, $W_{SCR} = W_{EPI}$ which, with Eq. (6) in [JEON87] and (2.3) for V_{BCI} (= V_{BCO} when $W_{QNR} = 0$) defines the relation between V_{BC} and I_C at the onset.

The complete dc solution for the carrier transport in the BJT is given implicitly in the model by equating the

current defined by the collector analysis, I^C_C from Section 2.2, to that defined by the base analysis, I^B_C from (2.10) in Section 2.3. Via the numerical Newton method, iterations yield the solution when $I^B_C \cong I^C_C$ to with in a specified tolerance. This solution also yields the quasi-static voltage dependences of the charges stored in the base and collector regions of the device.

The network representation of one-dimensional charge-based model is shown in Fig. 2.2. Q_N is the minority electron charge in QNB region, Q_{EE} is the hole charge stored in the quasi-neutral emitter region. Q_{JE} and Q_{JC} are the emitter- and collector-junction depletion charges respectively. Q_{QNR} is the excess electron charge in the current-induced SCR in the collector. Q_N and Q_{QNR} are partitioned between the emitter and collector terminals using two partition factors, f_B and f_C. The details of the charge, the partitioning of charges, and the base current are explained in Section 5.2.3.

2.5 Summary

The one-dimensional charge-based large-signal model which serves as the basis for the multi-regional charge-based model is explained. It is a very physical, semi-numerical model. The collector region modelling is an extension of

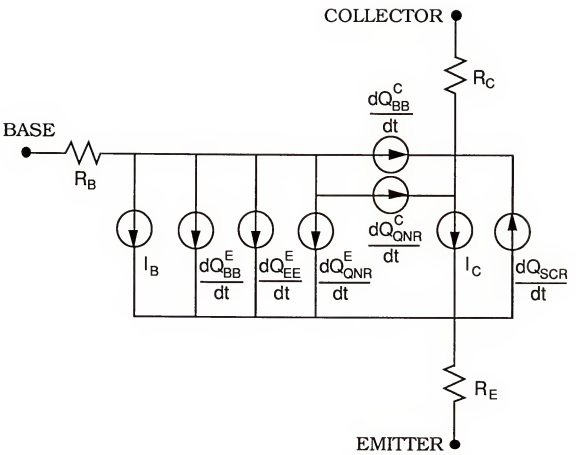


Fig. 2.2 Network representation of the charge-based bipolar npn transistor model.

Kull's quasi-saturation model and accounts for the current-induced SCR formation at sufficiently high-current densities. The base region model is analytical and assumes an exponential doping profile. The base-collector boundary conditions which link the base- and collector-region analysis are determined numerically. The one-dimensional model is not only used as an intrinsic transistor model in the multi-regional model, but the results are also used in the intrinsic base resistance model.

CHAPTER 3
INTRINSIC BASE RESISTANCE MODEL

3.1 INTRODUCTION

In Chapter 2, a one-dimensional charge-based model has been introduced which is to be expanded into a multi-regional charge-based model. In this chapter, a physical intrinsic base resistance model is developed which is self-consistent with the one-dimensional model and essential to the multi-dimensional composition of an advanced BJT. An accurate model for the intrinsic resistance is necessary for the multi-regional model because the voltage drop between the base of the peripheral and intrinsic transistor has to be consistent with the intrinsic base current flowing through this resistance and, thus, establishing the dc biases in the model.

In high-performance bipolar transistor applications, the intrinsic base resistance of the bipolar transistor is one of the critical elements in determining the internal bias conditions between the intrinsic bipolar transistor and its peripheral elements, the transistor switching speed and its small-signal frequency response. The functional dependence of the dc intrinsic base resistance on terminal voltages and

currents has been modeled and analyzed using several modeling approaches. Hauser [HAUS64] derived an analytic model for the intrinsic base resistance that included the two-dimensional (cross-sectional) emitter crowding effect at low currents. Luo and Graham [LUO87] inferred the intrinsic base resistance using an one-dimensional numerical computer simulation (SEDAN II) for each transistor in a two-dimensional matrix representation of the intrinsic transistor. Although this formulation of base resistance is valid over the entire current range, it is computationally complex and therefore difficult to use for circuit simulation. Hebert and Roulston [HEBE88] derived an empirical model from mask and sheet resistivity information using a two-dimensional computer simulation. This model for the intrinsic base resistance is only valid at low currents. Valsamakis [VALS86] derived an analytic two-dimensional model using the power method which is also only valid for low currents. The last three contributions were primarily concerned with the effect of small-area transistor geometries on the intrinsic base resistance.

At high currents, the variation of the voltage drop across the emitter-base junction, referred to as emitter crowding, the high injection effects in the base and collector, and base push-out become important. These three

effects tend to reduce the intrinsic base resistance. In self-aligned polysilicon-contacted bipolar transistors, the base of the intrinsic transistor is biased internally through the intrinsic base resistance relative to the peripheral transistor and extrinsic diode [REIN84]. Although the intrinsic base resistance may fall to a fraction of its low-current value, at high currents a large voltage drop can occur across this resistance, resulting in the debiasing of the intrinsic transistor from its peripheral elements. In order to model the multi-regional charge based BJT model, it is necessary to have a simple circuit model for the intrinsic base resistance that is valid for low and high current operation.

In this chapter, an analytic model for intrinsic base resistance is developed for low through high current operation. It is tailored to the highly physical one-dimensional charge-based large-signal bipolar transistor model [FOSS87], [JEON89]. This model includes high current effects in the base and collector region, that is, base push-out into the collector region and high-level injection, and it is semi-numerical. Hauser's model is expanded to include not just emitter crowding but also the effect of high injection and base push-out, which are derived from the charge-based large-signal model. The resulting model can

predict the effect of resistivity modulation which depends on conductivity modulation, current crowding and base push-out, on intrinsic base resistance for transistors of known doping profile in the base and collector and known emitter window dimensions. Unlike other models for intrinsic base resistance, this model is highly physical and has no empirically determined parameter explicitly in it (although the Jeong and Fossum model [JEON89] has empirical parameters). This new base resistance model is then verified using PISCES II and implemented using user-defined controlled sources (UDCS's) into SLICE [HARR84], an enhanced version of SPICE2. This results could be written into code in SPICE2 in the future

In Section 3.2, Hauser's model is explained with minor modification. The base resistance for single- and double-contact are derived. In Section 3.3, using the parameters extracted from the one-dimensional model, the base resistance model is completed. In Section 3.4, the base resistance model is verified with the aid of PISCES simulation.

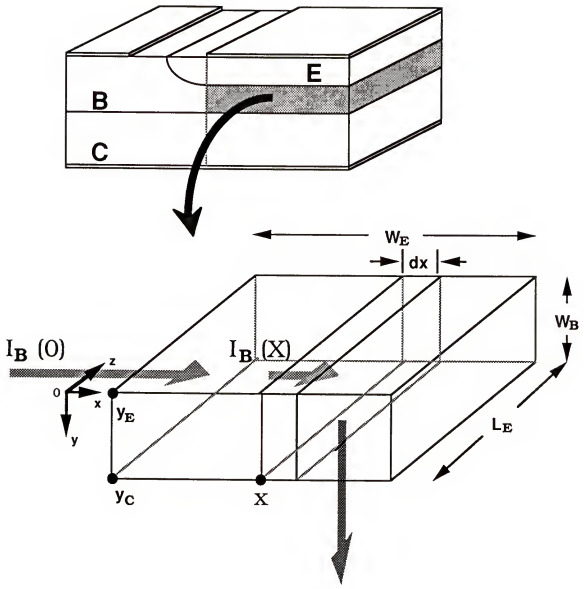
3.2 Hauser Model for Intrinsic Base Resistance Revisited

Hauser's model [HAUS64] is valid for the low current region where high-injection effects in the base and collector

and base push-out are unimportant. In expanding his model and adapting it for one-dimensional charge-based large-signal model for intrinsic base resistance, it is assumed that (1) the quasi-neutral-base thickness W_B, the pushed out quasi-neutral collector thickness W_{QNR}, and intrinsic QNB resistivity ρ_{BC}, and the current gain β are constant across the intrinsic base region, but are dependent on bias, and (2) the voltage drop in the emitter region and the base recombination are negligible. For strong emitter crowding, these assumptions are not generally valid but for the small geometries of advanced bipolar transistors, emitter crowding is not as significant an effect. Although this computational approach is the same as Hauser's, the values of W_T, ρ_{BC}, β, and N_{FC} are derived (shown in section 3.3) from the charge-based transistor model [FOSS87,JEON89].

A schematic of the intrinsic base resistance for a stripe-transistor geometry is given in Fig. 3.1. For a base resistance with thickness dx, the base current flows from the base contact into the intrinsic QNB such that a lateral variation in the voltage drop across the emitter-base junction appears from the end nearest the contact at x = 0 to the other side. This variation is

Fig. 3.1 Three dimensional structure of BJT with single base contact. The intrinsic quasi-neutral base region dimensions, and the base and collector currents are labeled.


E
B
C
W_E
dx
W_B
I_B (0)
I_B (X)
z
0
x
y
y_E
y_C
X
L_E
J_C (X) L_E dx

$$V_{BE}(x) = V_{BE}(0) - \int_0^x \frac{I_B(x)}{L_E\ W_T}\ \rho_{BC}\ dx \tag{3.1}$$

where L_E is the emitter length. Although this approach is similar to Hauser's, the base current is related to the collector current density $J_C(x)$ and current gain β in this case. The collector current density which flows through the intrinsic base region plate is

$$J_C(x) = J_0 - \exp\left(\frac{V_{BE}(x)}{N_{FC}\ V_T}\right) \tag{3.2}$$

where the ideality factor N_{FC} ($1 \leq N_{FC} \leq 2$) depends on the charge-based collector current and will be defined later, and V_T is the thermal voltage. N_{FC} is assumed to be independant of x which is a first-order approximation and may not valid for all transistor. Although this accounts for high-level injection, it does not take care of base push-out which is taken from the one-dimensional charge-based model. Following Hauser's approach (in [HAUS64], Eqs. (4)-(9)) with boundary conditions $I_B(W_E) = 0$ and $I_B(0) = I_B$, the solution for the base current is

$$I_B(x) = \frac{2N_{FC}V_T L_E W_T}{\rho_{BC} W_E}\ Z\ \tan\left[Z\left(1 - \frac{x}{W_E}\right)\right] \tag{3.3}$$

where W_E is the emitter window dimension given in Fig. 3.1 and where Z is obtained from the relationship

$$Z \tan Z = \frac{\rho_{BC} W_E}{2 N_{FC} V_T} \frac{I_B}{L_E W_T}. \tag{3.4}$$

The equivalent intrinsic resistance is then calculated by the power dissipation method, an identical approach to Hauser's. It is

$$R_{BI} = \frac{\rho_{BC} W_E}{L_E W_T} \left[\frac{\tan Z - Z}{Z \tan^2 Z} \right]. \tag{3.5}$$

This case is for a single-base contact. For a double-base contact, $I_B (-W_E/2) = -I_B (W_E/2) = I_B/2$ and, using the same approach, the double-base contacted resistance is

$$R_{BI} = \frac{1}{4} \frac{\rho_{BC} W_E}{L_E W_T} \left[\frac{\tan Z - Z}{Z \tan^2 Z} \right] \tag{3.6}$$

where

$$Z \tan Z = \frac{\rho_{BC} W_E}{8 N_{FC} V_T} \frac{I_B}{L_E W_T} \tag{3.6a}$$

The resulting intrinsic base resistance depends on four bias-dependent quantities ρ_{BC}, I_B, W_T, and N_{FC}. The derivation of

the bias-dependence for these quantities as they are taken from the one-dimensional model will be presented in Section 3.3.

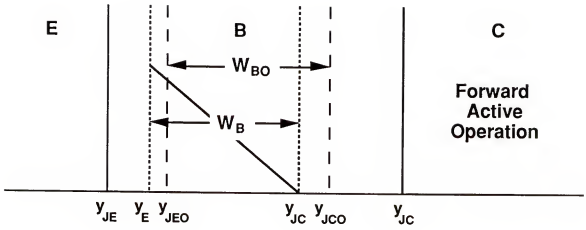
3.3 Extended Intrinsic Base Resistance Model

The base current I_B, the collector current I_C, the excess charges is the base and collector regions at high currents, and the effective base width W_T are taken directly from the output of the large-signal charge-based model [JEON87]. W_T is the sum of the normal base width W_B and the extension of the QNB into the collector W_{QNR} at high currents(see Fig. 3.2).

The ideality factor N_{FC} which accounts for the collector current level in Eq. (3.2) is derived from the formulation of the collector current in the charge-based model. The exponential dependence in Eq. (3.2) can be expressed as

$$\exp\left(\frac{V_{BE}}{N_{FC}V_T}\right) \cong \frac{N_{AE}\exp\left(\frac{V_{BE}}{V_T}\right) + C_F\, n_E \exp\left(\frac{V_{BE}}{2V_T}\right)}{N_{AE} + C_F\, n_E} \qquad (3.7)$$

and



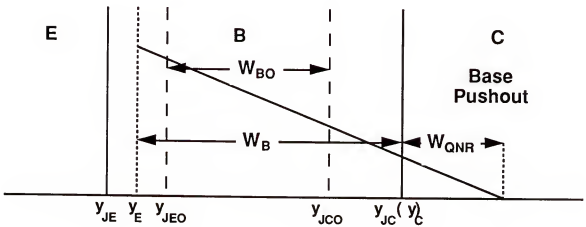


Fig. 3.2 The excess electron concentrations for an npn transistor (a) in forward active region (V_{BE} > 0V, V_{BC} < 0V) and (b) in quasi saturation region (V_{BE} > 0V, V_{BC} > 0V). y_{JE} and y_{JC} are the metallurgical junction locations and y_{EO} and y_{CO} are QNB boundary locations at equilibrium. The excess electron concentration pushes out into the collector in (b) resulting in a total base width W_T equal to the sum of W_B and W_{QNR}.

$$\frac{1}{N_{FC}} \equiv \frac{V_T}{V_{BE}} \ln\left(\frac{N_{AE} \exp\left(\frac{V_{BE}}{V_T}\right) + C_F\, n_E \exp\left(\frac{V_{BE}}{2V_T}\right)}{N_{AE} + C_F\, n_E}\right) \tag{3.8}$$

where V_{BE} is the average voltage drop across the emitter-base junction in the charge-based model. (See Fig. 3 in [JEON87].) N_{FC} varies between 1 and 2 depending on injection level. In low injection, ($n_E << N_{AE}$)

$$\frac{1}{N_{FC}} \equiv \frac{V_T}{V_{BE}} \ln\left(\frac{N_{AE} \exp\left(\frac{V_{BE}}{V_T}\right)}{N_{AE}}\right) = 1. \tag{3.9}$$

In high injection, ($n_E >> N_{AE}$)

$$\frac{1}{N_{FC}} \equiv \frac{V_T}{V_{BE}} \ln\left(\frac{C_F\, n_E \exp\left(\frac{V_{BE}}{2V_T}\right)}{C_F\, n_E}\right) = \frac{1}{2}. \tag{3.10}$$

The intrinsic base resistivity can be defined as the inverse weighted average of the conductivities of the quasi-neutral base region and the extension of the base into the collector [GRAY77],

$$\rho_{BC} = \frac{W_T}{\int_{W_T} q\, \mu_p(y)\, p(y)\, dy}$$

$$= \frac{W_B + W_{QNR}}{\int_{W_B} q\ \mu_p(y)\ p(y)\ dy + \int_{W_{QNR}} q\ \mu_p(y)\ p(y)\ dy} \qquad (3.11)$$

where W_T is described above, p is the hole concentration, and the hole mobility μ_p depends on dopant concentration. The derivation of the intrinsic base resistivity then depends on the hole concentration in the base and collector which is bias dependent. (In low injection, the hole concentration is equal to the base dopant concentration as in Eq. (3.13) and in high injection, it is derived from the output of the charge-based model as in Eq. (3.15).) It also depends on the hole mobility which depends on the doping concentration for low and high injection (the carrier-carrier scattering effect on mobility is assumed negligible.). The hole mobility can be approximated as (see Fig. 3.3)

$$\mu_p = C_A - C_B \ln(N_A) \qquad (3.12)$$

where N_A is in cm^{-3}, C_A = 2800 $cm^2/Vsec$ and C_B = 65.14 $cm^5/Vsec$. This approximation is only valid when peak base doping concentration is less than 10^{18} cm^{-3}. However, for most BJT, this assumption is applicable. In low injection, $n(y) \ll N_A(y) \cong p(y)$ and, using Eqs. (2.6) and (3.12),

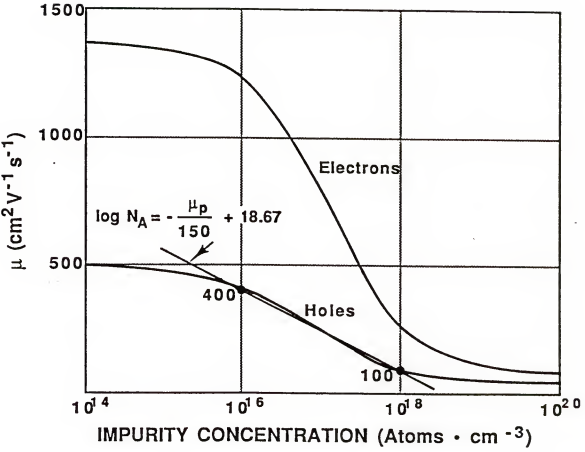


Fig. 3.3 Electron and hole mobilities in silicon at 300K as a function of the total dopant concentration. An approximation for the hole mobility in the base region is shown. N_A is in cm^{-3} and μ_p is in cm/Vsec.

$$\int_{y_E}^{y_C} q\,\mu_p(y)\,p(y)\,dy \cong \int_{y_E}^{y_C} q\,\mu_p(y)\,N_A(y)\,dy$$

$$= \frac{q\,C_B\,N_{AO}\,W_{BO}}{\eta}\left[\frac{\eta\,y_E}{W_{BO}} + \frac{C_A}{C_B} - \ln\,(N_{AO})\right]\exp\left(-\frac{\eta\,y_E}{W_{BO}}\right)$$

$$- \frac{q\,C_B\,N_{AO}\,W_{BO}}{\eta}\left[\frac{\eta\,y_C}{W_{BO}} + \frac{C_A}{C_B} - \ln\,(N_{AO})\right]\exp\left(-\frac{\eta\,y_C}{W_{BO}}\right) \qquad (3.13)$$

where N_{AO} is in cm^{-3}. In high injection, $n(y) >> N_A(y)$ and $p(y) \cong n(y)$ which is taken from the excess base charges in the charge-based model. By integrating Eq. (2.7) from y_E to y,

$$n(y) = n(y_E) + \frac{I_C}{2qA\overline{D_n}}\,(y - y_E) \qquad (3.14)$$

where $\overline{D_n}$ is taken from the charge-based model [JEON89]. Then using Eqs. (2.6), (3.12), and (3.14),

$$\int_{y_E}^{y_C} q\,\mu_p(y)\,p(y)\,dy \cong \int_{y_E}^{y_C} q\,\mu_p(y)\,n(y)\,dy$$

$$= \frac{I_C C_B}{2A\overline{D_n}}\left\{\frac{\eta}{3W_{BO}}\,W_B^{\,3} + \left[\frac{C_A}{C_B} - \ln\,(N_{AO}) - \frac{\eta y_E}{W_{BO}} + \frac{2qA\overline{D_n}\eta}{I_C W_{BO}}\,n(y_E)\right]\frac{W_B^{\,2}}{2}\right\}$$

$$+ \frac{I_C C_B W_B}{2A\overline{D_n}} \left[\frac{C_A}{C_B} - \ln\left(N_{AO}\right)\right] \left[- y_E + \frac{2qA\overline{D_n}\eta}{I_C}\, n(y_E)\right] \tag{3.15}$$

where $W_B = y_C - y_E$. The intrinsic base resistivity at high currents depends on this term and

$$\int_{W_{QNR}} q\, \mu_p(y)\, p(y)\, dy = \mu_p(N_{EPI})\, \frac{Q_{QNR}}{A} \tag{3.16}$$

where Q_{QNR} is derived directly from the charge-based model [JEON87] and its dependence on epitaxial dopant concentration is given in Eq. (11) in [JEON87] and the pushed-out base width is given in Eq. (7) in [JEON87].

3.4 Verification of the Intrinsic Base Resistance Model and Discussion

The verification of our intrinsic base resistance model is done two ways. First the hole concentration and mobility, the base current, the effective base width and injection level taken from PISCES II [PINT84] are input into Eqs. (3.4) and (3.5). The base resistance derived from the power method also using PISCES II is compared to that in Eq. 3.5. Then the base resistance is calculated using the charge-based large-signal transistor model outputs in Eqs. (3.4), (3.5), (3.8),

(3.11), and (3.12) and this is compared with the PISCES II simulation.

To carry out the first verification, the base region is broken up into the intrinsic and peripheral regions as shown in Fig. 3.4(a). (The coordinate x_o defines the boundary between the intrinsic and peripheral transistors in this figure.) The mesh is exaggerated in this figure in order to explain the derivation of the base current and power dissipated in the intrinsic base region. The box represents the two-dimensional area around each mesh point. The box dimensions are defined by the adjacent mesh spacings. For example, the box dimensions surrounding the mesh point x_i, y_j are

$$L_{x_i} = \frac{x_{i-1} - 2x_i + x_{i+1}}{2}$$

$$L_{y_j} = \frac{y_{j-1} - 2y_j + y_{j+1}}{2} \qquad (3.17)$$

where x and y are defined in Fig. 3.4(a). The base current (that is, the base current per unit length in the third dimension) entering the intrinsic region

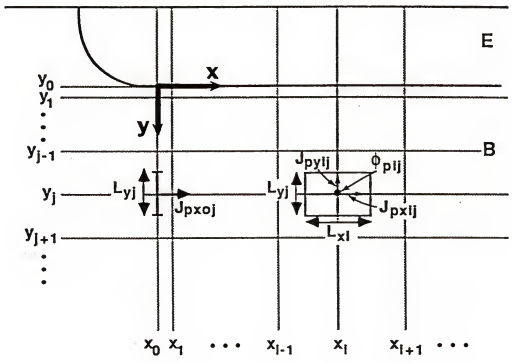


Fig. 3.4(a) The mesh structure of BJT for PISCES II simulation. The coordinate x_o divides the transistor intrinsic region from periphery. Jpx_{ij} and Jpy_{ij} are hole current density at mode (x_i, y_j) for x and y direction. Lx_i and Ly_i are the dimensions of the box for which the power loss is calculated.

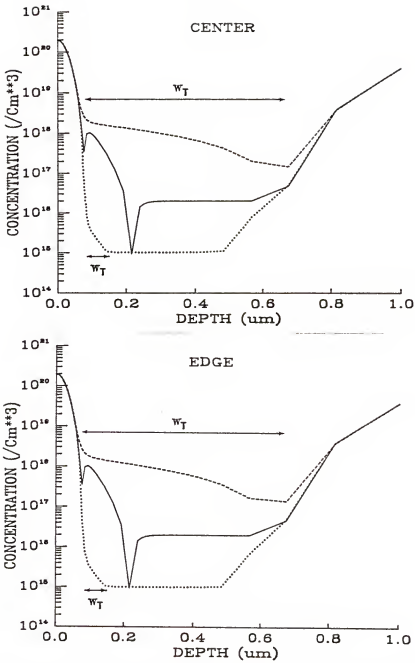


Fig. 3.4(b) The cross-sectional doping (———) and electron concentrations at V_{BE} = 0.8V (····) and at V_{BE} = 1.0V (----) for V_{BC} = -2V The first figure is taken at the center of the emitter and the second one is taken at the edge of the intrinsic emitter. The effective base width W_T is shown.

$$I_{BT}(x_0) = \int_{W_B} J_p \, dy \, \hat{x} = \int_{W_B} \left(J_{px_{0j}} \, \hat{x} + J_{py_{0j}} \, \hat{y} \right) dy \, \hat{x} = \sum_j J_{px_{0j}} \, L_{y_j} \, . \tag{3.18}$$

The power (the power per unit length) consumed at each mesh point is

$$P_{ij} = \left| J_{px_{ij}} \, L_{y_i} \, \frac{\phi_{P_{i+1,j}} - 2 \, \phi_{P_{ij}} + \phi_{P_{i-1,j}}}{2} \right| + \left| J_{py_{ij}} \, L_{x_i} \, \frac{\phi_{P_{i,j+1}} - 2 \, \phi_{P_{ij}} + \phi_{P_{i,j-1}}}{2} \right| . \tag{3.19}$$

The total power consumed in the intrinsic base region is the sum:

$$P_T = \sum_i \sum_j P_{ij} \tag{3.20}$$

and the intrinsic base resistance can be calculated by the power method:

$$R_{BI} = \frac{P_T}{I_{BT}^2} . \tag{3.21}$$

The verification of the analytic model for R_{BI} by PISCES II simulation uses the computation of the average base

resistivity as a function of injection level. This is done by inputting the carrier concentration and mobility at each mesh point into the formulation for the resistivity

$$\rho_{BC} = \frac{W_E W_T}{\int_{W_E}\int_{W_T} q\ \mu_p(x_i, y_j)\ p(x_i, y_j)\ dx\ dy} \tag{3.22}$$

where W_T is the effective base width taken from PISCES II and W_E is the emitter width.

In Section 3.2, it is assumed that N_{FC}, β, ρ_{BC}, W_T are independent of x. In Fig. 3.4(b), the PISCES simulation of the electron density as a function of depth (y-direction) is given for two different x-position, one at the center of the emitter and one at the edge of the intrinsic region ($x = x_o$ in Fig. 3.4(a)). It can be seen that the injection level and the effective base width W_T are independent of x. This implies that N_{FC} and ρ_{BC} are also independent of x. The assumption that β is independent of x is not valid when emitter crowding is important, but, from the results that follow, it does not appear to be a significant effect for our transistor.

In Fig. 3.5, the PISCES II-derived R_{BI} using the power method is compared with the model given in Eqs. (3.4) and (3.5). The one-dimensional dopant profile for both the

PISCES II- and the one-dimensional charge-based transistor model simulations is given in Fig. 3.4(b). At low current, there is a 10% difference between the R_{BI} simulated by these two different ways which we attribute to the limitation of mesh point in PISCES II needed for convergence. However, at low currents the voltage drop across R_{BI} which is the difference in the voltage drops across the peripheral and intrinsic transistor base-emitter junction is negligible. At high currents, where the voltage drop across R_{BI} is important, the agreement is very good. (Emitter crowding is not insignificant for transistors of these sizes. The collector current density at the boundary between the intrinsic and peripheral transistor at the base-collector junction is ~ 1.8 times that at the center of the intrinsic transistor for V_{BE} = 0.95 V from PISCES II simulations.) In the second verification, R_{BI} is implemented as a current source into UDCS in SLICE. THE UDCS representation is well explained in Ref. [JEON87] Section IV. The charge-based large-signal transistor model current sources generates the parameters W_T, I_B, and I_C. With these parameters and process- (N_{AO}, Z, W_{BO}, N_{EPI}) and layout-related parameters (W_E and L_E); ρ_{BC} (see Eq. (3.11), (3.13), (3.15), and (3.16)); Z (see Eq. (3.4) or (3.6)); N_{FC} (see Eq. (3.8)); and R_{BI} (see Eq. (3.5) or (3.6)) are calculated. The current source for R_{BI} supplies I_{RBI},

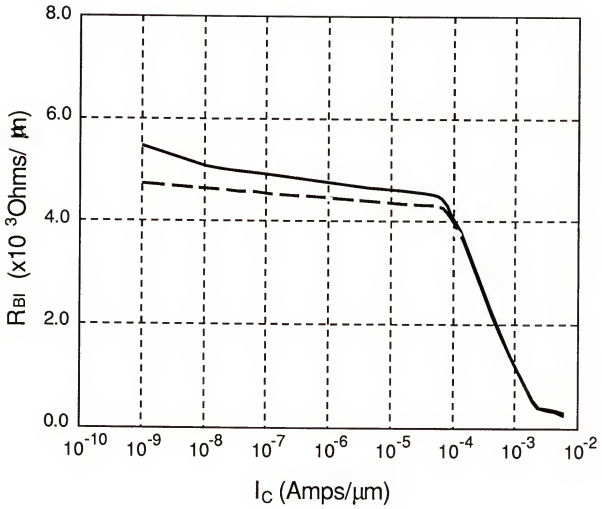


Fig. 3.5 PISCES II simulated R_{BI}(———) and SLICE-calculated RBI (----) as a function of collector current I_C (V_{BC} = -2V) using Eqs. (3.4) and (3.5) for a 1.2 μm emitter width BJT. The units of collector current (A/μm) and R_{BI} (Ohms/μm) refer to normalized values to the emitter length L_E in the third dimension.

$\partial I_{RBI}/\partial V_{BE}$ and $\partial I_{RBI}/\partial V_{BC}$ to SPICE2 which solves the nodal analysis for the charge-based large-signal model.

The SLICE simulation of R_{BI} is compared with the PISCES II simulation in Fig. 3.6 for a transistor with double-base contacts and emitter window 1.2 X 3.2 μm^2. (The emitter window dimensions are not fitting parameters in our simulations but are taken directly from layout information.) The PISCES II simulation for the peripheral transistor base resistance R_{BP} and the extrinsic p^+/n junction base resistance R_{BX} is also given for this transistor. The peripheral region R_{BP} has a similar functional dependence as R_{BI} on bias, but it is smaller in magnitude when compared to R_{BI}. It is assumed that $R_{BP} + R_{BX}$ is constant in the model which is accurate for the current range of interest.

In Fig. 3.7, the functional dependence of R_{BI}, W_T, ρ_{BC}, and Z on bias for 1.2 X 3.2 μm^2 emitter window is given. These data are taken from the R_{BI} derived using the one-dimensional charge-based transistor model. R_{BI} decreases slightly at low V_{BE} because of the late-effect (decreasing emitter-base space-charge-region width). R_{BI} then decreases more rapidly (for V_{BE} = 0.85 V) as the emitter crowding factor begins to rapidly increase (for V_{BE} > 0.75 V in Fig. 3.7(a)) as the base region pushes out into the epitaxial collector (seen as an increase in W_T for V_{BE} > 0.9 V in Fig. 3.7(a)),

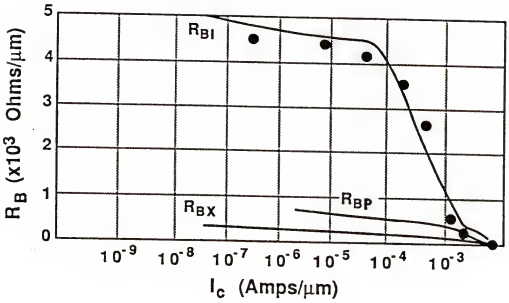


Fig. 3.6 PISCES II simulated base resistances R_{BX} (extrinsic p^+/n junction base resistance), R_{BP} (peripheral transistor base resistance), and R_{BI} (intrinsic region base resistance) for 1.2 μm emitter width. The simulated data (●) using SLICE are normalized to unit length (1 μm). In the SLICE simulation R_{BP} = R_{BX} are assumed to be constant and much smaller than R_{BI}.

and the base resistivity decreases as higher injection levels are reached (seen as a decrease ρ_{BC} for $V_{BE} > 0.9$ V in Fig. 3.7(b)). The emitter crowding factor Z increases with V_{BE} until $V_{BE} > 0.9$ V when the base resistivity and the base push-out dominate.

Some error is introduced into the model for R_{BI} in Eq. (3.6) because of computational inadequacies in the large-signal model. There can be slight discontinuities in the currents, in the voltages, and the boundary conditions internal to the model in the operating region between low and high collector current. (See the discussion in Section II.C Ref. [JEON89].) In Fig. 3.7(b) the emitter crowding factor Z monotonically increase with I_B. However, this crowding factor begins to decrease around $V_{BE} = .85$ V. At this bias point, W_T and ρ_{BC} dominate in Eq. (3.4).

3.5 Summary

A physical model for the intrinsic base resistance is developed which includes emitter crowding, conductivity modulation and base push-out. Therefore, this model is valid not only for low current, but also for high current region. It can be used in the multi-regional charge-based large-signal model. The model is implemented into UDCS in SLICE, and verified with PISCES simulation.

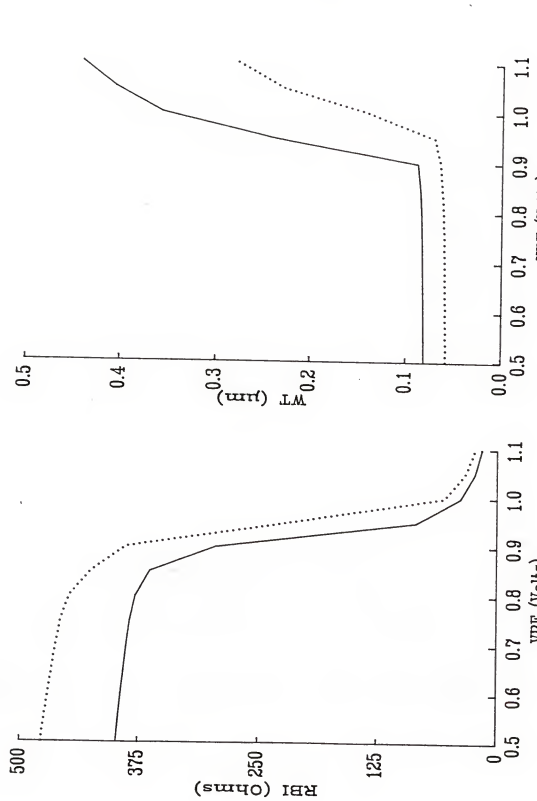


Fig. 3.7(a) R_{BI} and parameters W_T are simulated using SLICE for 1.2 X 3.2 μm^2 emitter area for V_{BC} = 0 V (____) and V_{BC} = -2 V (....).

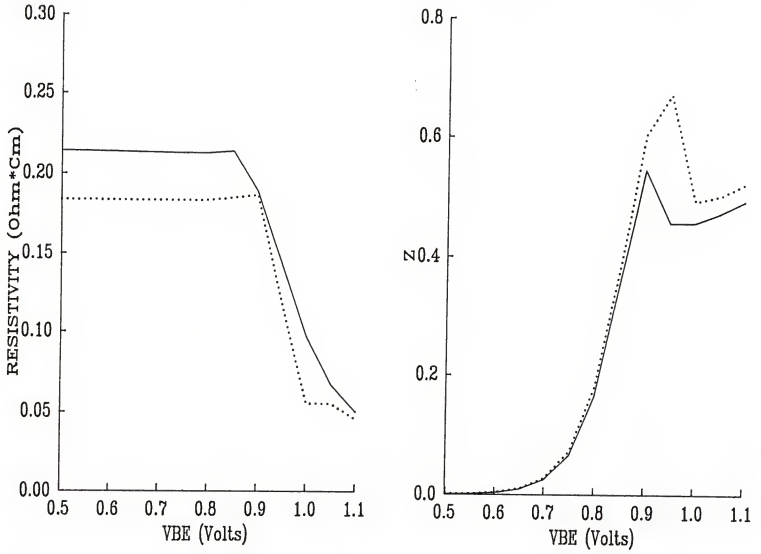


Fig. 3.7(b) ρ_{BC}, and Z are simulated using SLICE for 1.2 X 3.2 μm2 emitter area for V_{BC} = 0 V (____) and V_{BC} = -2 V (....).

CHAPTER 4
SEPARATION OF JUNCTION CAPACITANCE

4.1 Introduction

To accurately model the distributed, multi-dimensional characteristics of the bipolar transistor as a function of frequency, it is necessary to separate the bias-dependant base-collector and emitter-base junction capacitances between the intrinsic and peripheral regions of the device structure (see Fig. 4.1).

In this chapter such a technique for separating junction capacitances is presented which is the corollary of the H. M. Rein approach for separating the base and collector currents [REIN84]. The proposed technique has the advantage that no separate calibration step is needed to subtract out the contact pads and interconnect parasitic capacitances from the measured data. A three-step approach is outlined for extracting (1) the zero-bias intrinsic and peripheral junction capacitances, (2) the built-in potential and power dependence for the equivalent bias-dependent capacitances and (3) the corner capacitance of the peripheral transistor and the parasitic capacitance by using transistors with different emitter areas. The underlying assumptions in this approach

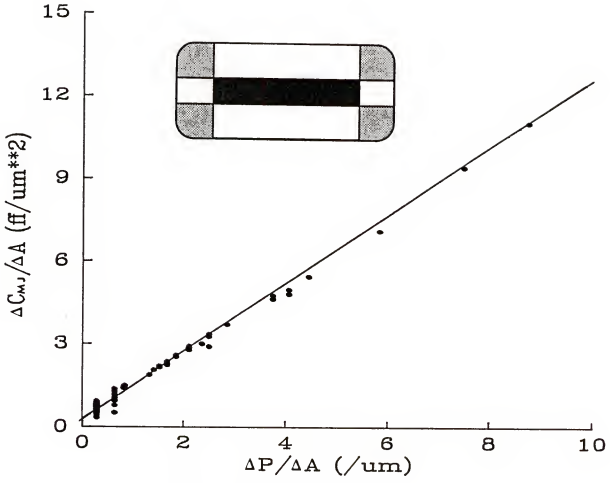


Fig. 4.1 Eq. (4.2) is plotted for the zero-bias base-collector junction capacitances (dots). The least square fit (solid line) yields a slope C_{JCOP} = 1.25 fF/μm and an intercept C_{JCOI} = 0.44 fF/μm. The extracted C_{JCOP}, and C_{JCOI} are used as initial values for the step 2. The top view of the transistor is given in the inset. The emitter window ($A \cdot C_{JCOI}$) is in black; the four corner regions ($4 \cdot C_{CNR}$) are in grey; and the peripheral region excluding the four corners ($P \cdot C_{JCOP}$) is in white.

are (1) the intrinsic and peripheral capacitance /um2 and /um, respectively, are independent of the size of the emitter window, (2) the built-in potential and the voltage-dependence for the two capacitances are identical and (3) the corner capacitances are the same for all transistors.

In Section 4.2, the extraction technique and experiment procedure is explained step by step. In Section 4.3 it is shown through the goodness of fitting the measured capacitances as a function of bias that this approach is generally valid for base-collector junction capacitances and we discuss its utility for the emitter-base region.

4.2 Experiment and Separation Technique

The junction capacitance as a function of bias for the advanced double-polysilicon self-aligned bipolar transistor with varying drawn emitter areas (1, 1.25, 1.5, 1.75, 2, 3 X 4 and X 8 μm^2) has been measured using an HP4194A Impedance Gain Analyzer on-wafer. The Impedance Analyzer is very accurate with a reported error for 0.15% for impedance measurements [HEWL88]. To demonstrate the separation technique, we will refer to the base-collector junction capacitance as a function of bias for the jth device as

$$C_{MC}^{j} = \left[A^{j}\ C_{JCOI} + P^{j}\ C_{JCOP} + 4\ C_{CCNR}\right]\left[1 + \frac{|V_{BC}|}{\phi_C}\right]^{m_C} + C_{PRS} \tag{4.1}$$

where A is the emitter window area which is smaller than the drawn dimension because of the oxide spacer (~ 0.4 μm) which is taken from the cross-sectional scanning electron micrographs [ZDEB87]; P is its peripheral length; C_{JC0I} and C_{JCOP} (/μm² and /μm, respectively) are the zero-bias intrinsic and peripheral base-collector junction capacitances which we assume have the same built-in barrier height ϕ_C, power m_C, and bias V_{BC}, C_{CNR} is the capacitance at one corner of the peripheral region and C_{PRS} is the parasitic capacitance.

The first step is to extract C_{JCOI} and C_{JCOP} by taking the differences between the measured capacitances of different known emitter areas at zero bias. The result of this procedure is plotted in Fig. 4.1 and given by

$$\frac{C_{MC}^{i} - C_{MC}^{j}}{A^{i} - A^{j}} = \left[\frac{P^{i} - P^{j}}{A^{i} - A^{j}}\right] C_{JCOP} + C_{JCOI} \tag{4.2}$$

where $A^{i} > A^{j}$. The slope of the linearly- fitted line is C_{JCOP} and the y-axis intercept is C_{JCOI}.

The second step is to extract the built-in potential ϕ_C and the power m_C from the measured data over the bias range of interest. This is accomplished by summing over the

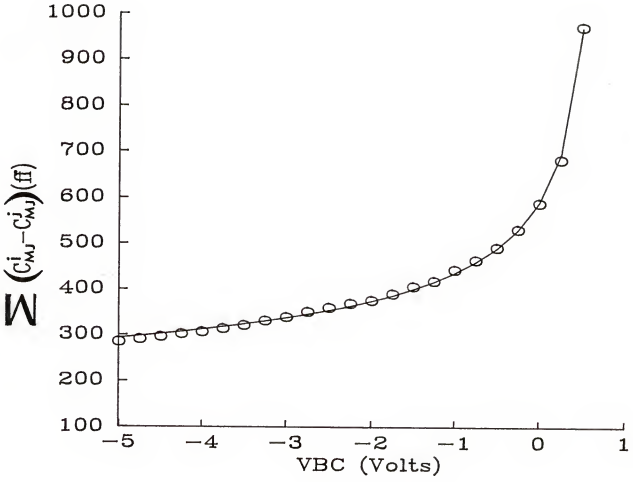


Fig. 4.2 The sum (~ 13!) over all the differences in the measured base-collector junction capacitances as a function of bias (O) is given. From the non-linear least square fit (——), ϕ_C = 0.66V and m^C = 0.34 for our transistors.

differences between the measured data for two different devices and plotting this sum as a function of bias. The formula is as follows:

$$\sum_j C_{MC}^j = \sum_j \left[A^j\ C_{JCOI} + P^j\ C_{JCOP}\right] \left[1 + \frac{|V_{BC}|}{\phi_C}\right]^{m_C} . \qquad (4.3)$$

A nonlinear least square fit (the Levenberg-Marquardt method [PRES86]) is then used to extract the values of ϕ_C and m_C. The summation and the fit for our devices are given in Fig. 4.2.

The third step is to add all the measured capacitances together as a function of bias and fit the results using Eq. (4.4), the nonlinear least square fit algorithm in the second step, and the extracted values for C_{JCOI}, C_{JCOP}, ϕ_C and m_C from above in order to extract C_{CNR} and C_{PRS}. The values we obtain for C_{CNR} and C_{PRS} for our devices are 1.34 and 171 fF, respectively. This parameter extraction routine is programmed in FORTRAN language and is given in Appendix A.

4.3 Results and Discussion

The results of this technique are presented in Fig. 4.3. In this figure, eight different transistors having different emitter areas are fit using Eq. (4.1) with the six extracted

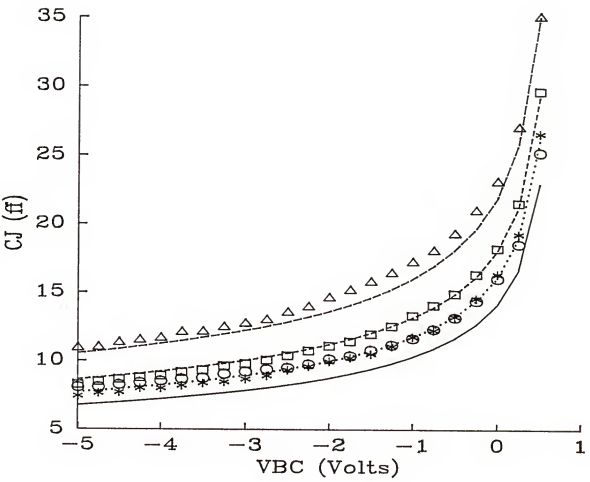


Fig. 4.3(a) The result (C_{MC} - C_{PRS}) of the three-step analysis for transistors having emitter areas (drawn emitter areas) 1 X 4 (o,____), 1.5 X 4 (*,···), 2 X 4 (˙,---), 3 X 4 μm^2 (Δ,- - -). The first symbols in the parentheses are measured data and the second lines are simulated data.

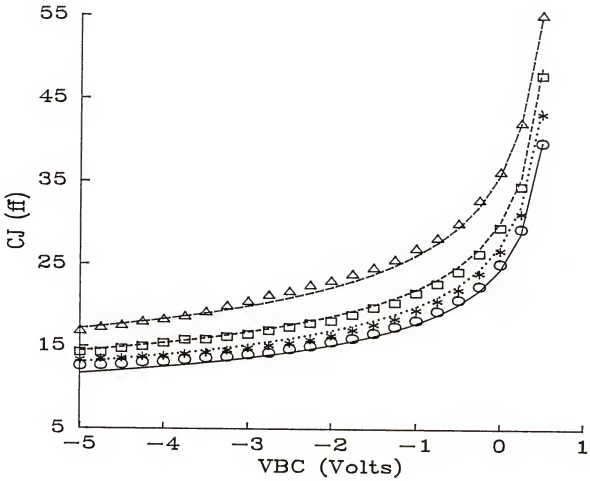


Fig. 4.3(b) The result (C_{MC} - C_{PRS}) of the three-step analysis for transistors having emitter areas (drawn emitter areas) 1 X 8 (o,___), 1.5 X 8 (*,···), 2 X 8 (˙,---), 3 X 8 μm^2 (Δ,- - -). The first symbols in the parentheses are measured data and the second lines are simulated data.

parameters given above. Except for two devices having emitter areas 1 and 3 X 4 μm^2, the fit to the measured capacitances is extremely good. The discrepancies between the fit and the measurement data for the 1 and 3 X 4 μm^2 devices is attributed to the assumptions of invariant parameters independent of emitter area and process variation. Measurement error is not a factor in any of the above discrepancies because, although the junction capacitance extracted using this technique (as well as other calibration techniques [PARK88]) is the difference of two large capacitances, $C_{MC} - C_{PRS}$, the measurement error is roughly 1.5% of its value. In addition, the total measured zero-bias junction capacitances are in good agreement with the results reported in [PARK88] on identical transistors. A more significant source of error may be the extraction of the corner capacitance C_{CNR} which is roughly 50 - 60% of the total extrinsic-region capacitance and roughly ten times larger than the total intrinsic capacitance for measured devices.

It is expected that the extracted parameters will vary from those extracted by other techniques, but this technique is supported by a large number of device measurements only some of which are reported here. This technique does not require a calibration procedure using dummy contact pads

without a transistor [PARK88] which are typically not the same size as the ones for the device under test.

Eq. (4.1) and the proposed approach may be less accurate when extracting parameters for the emitter-base junction capacitance because (1) this junction is often under forward bias and a more complicated expression for junction capacitance is needed [LIOU87], and (2) for reverse-bias, the assumption about identical voltage dependence for the intrinsic and peripheral may be less true. In this latter case, the approach presented here may still be valid if different ϕ and m are used for the peripheral transistor.

4.4 Summary

A technique which separates the base-collector and emitter-base junction capacitance between the different regions in the multi-regional model has been developed. To complete the multi-regional charge-based large-signal model, the emitter-base junction capacitance is divided between the intrinsic and the peripheral region, and the base-collector junction capacitance is divided into intrinsic, peripheral, and extrinsic regions. This experimental technique does not require calibration of parasitics. The capacitance model parameters are extracted using a three step process. The first step extracts C_{JOI} and C_{JOP}. The second step bias-

dependent measurement is used to extract the parameters ϕ and m. The third step is to extract the corner capacitance and the parasitic capacitance. The three step process is automated using FORTRAN program which is shown in Appendix A. This technique is used to extract the capacitances of different-d transistors, and is very accurate method.

CHAPTER 5
MULTI-REGIONAL CHARGE-BASED SMALL-SIGNAL BJT MODEL

5.1 INTRODUCTION

In Chapter 3 and 4, an intrinsic base resistance model compatible with the one-dimensional charge-based model and a technique for separating the junction capacitances between intrinsic and extrinsic transistor regions have been introduced. With the completion of these tasks, the complete multi-regional charge-based BJT model is developed in this chapter. The one-dimensional charge-based model in Chapter 2 is extended to include the peripheral parasitic BJT formed in the region linking the emitter-base junction to the extrinsic base and the extrinsic p^+/n base-collector (diode) junction capacitance.

In Section 5.2, the peripheral BJT charges and currents are related to the equivalent intrinsic transistor terms with the constants of proportionality taken from the layout geometry and empirical fitting parameters. The empirical fitting parameters which define the relationship between the peripheral and intrinsic region collector and base currents as a function of bias are taken from an approach by H. M. Rein [REIN87]. As explained in Chapter 3, the model for the

intrinsic base resistance is taken from an extension of Hauser's model includes emitter crowding effect, high injection effects in the base and collector and base push-out. The extraction of the other parameters such as contact resistances are also discussed.

In Section 5.3 a multi-regional charge-based small-signal model is fully developed using the large-signal model. The small-signal model equivalent circuit, derived from large-signal model, is given.

5.2 Multi-Regional Charge-Based Large-Signal Model and Parameters

A schematic of the multi-regional large-signal currents and charges is given in Fig. 5.1. This model is at present incorporated into SLICE in user-defined-control-sources and will be directly incorporated into SPICE2 source code for use in mixed-mode device/circuit simulation. The relationships between the intrinsic and peripheral transistor currents and charges, the extrinsic p^+/n diode, and the parasitic resistances will be discussed in the next section. In Fig. 5.2, the geometric and equivalent circuit representations emphasize the differences between the intrinsic and peripheral transistors.

These transistors have a common emitter and collector

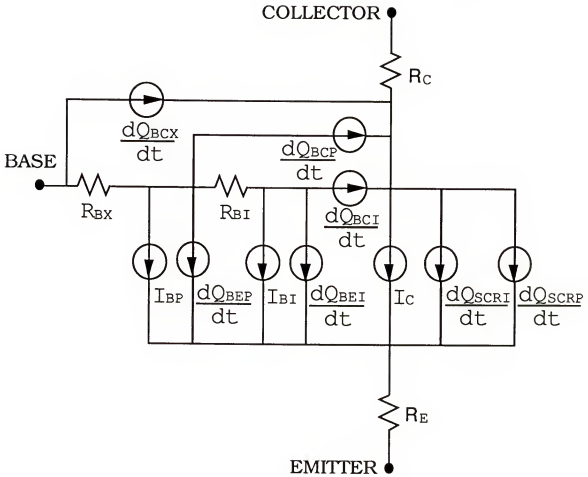
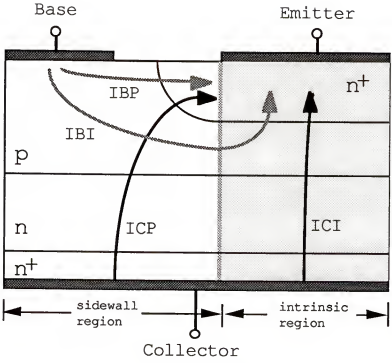
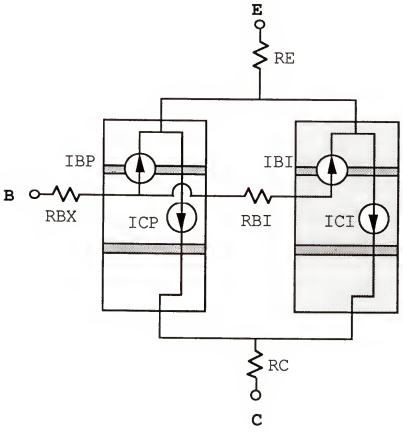


Fig. 5.1 A network representation of the multi-regional charge-based large-signal model. The subscripts for intrinsic transistor, the peripheral transistor, and the extrinsic base-collector junction are I, P, and X respectively.

Fig. 5.2 The geometric and circuit representations for the intrinsic (subscript I) and peripheral (subscript P) transistor. The intrinsic transistor's lateral boundaries are defined at the edges of the polysilicon contact to the emitter.


Base
Emitter
IBP
IBI
n+
p
n
ICP
ICI
n+
sidewall region
intrinsic region
Collector


E
RE
IBP
IBI
B
RBX
ICP
RBI
ICI
RC
C

terminal, but the potential at the base of the peripheral transistor is offset from the base of the intrinsic one by the potential drop across the intrinsic base resistance, R_{BI}, defined in Chapter 3. The edge of the polysilicon contact, fabricated in the emitter window opening, marks the boundary between the intrinsic and peripheral transistor regions. The extrinsic base resistance R_{BX}, the emitter resistance R_E and the collector resistance R_C are assumed constant. Most of the one-dimensional model parameters and the procedures for their extraction have already been given in Ref. [JEON89]. However, the emitter base and base-collector junction capacitances and the five additional parameters needed for the multi-regional model are presented next and the procedure for their extraction is explained in the following sections.

5.2.1 Collector Current Model

The complete definition of the collector current for low and high injection and for normal, quasi-saturation, and inverse mode operation for the intrinsic transistor is given in Eqs. (8) - (10) in [JEON89]. To show the relationship between the intrinsic and peripheral transistor currents, the same approach as by H. M. Rein [REIN84] is used, but more generally valid expressions for the total collector current

I_C the intrinsic and peripheral collector currents I_{CI} and I_{CP} are

$$I_C = I_{CI} + I_{CP} \tag{5.1}$$

$$I_{CI} = A\ C_I \left[\exp\left(\frac{V_{BE}}{V_T}\right) - \exp\left(\frac{V_{BCO}}{V_T}\right)\right] \tag{5.2}$$

$$I_{CP} = P\ C_P \left[\exp\left(\frac{V_{BEP}}{V_T}\right) - \exp\left(\frac{V_{BCOP}}{V_T}\right)\right] \tag{5.3}$$

where $V_{BCOP} - V_{BCO} = V_{RBI}$, the voltage drop across the intrinsic base resistance and

$$\frac{C_P}{C_I} = \frac{\overline{D_{NP}}}{\overline{D_{NI}}} \frac{G_I}{G_P} W_{EP} . \tag{5.4}$$

This ratio is the product of the ratio of average diffusivities $\overline{D_{NI}}$ and $\overline{D_{NP}}$ and of the Gummel numbers G_I and G_P for the intrinsic and peripheral base regions, respectively; W_{EP} is the length of the emitter junction at the sidewall in the peripheral transistor (see Fig.5.2); V_{BE}, V_{BEP}, V_{BCO}, and V_{BCOP} are the respective quasi-Fermi-level separations across the emitter-base and base-collector space-charge-regions (SCR) as in [JEON89]. Using the Rein approach, the intrinsic and peripheral current components are redefined to have

explicit dependencies on the emitter window area A and the total emitter window peripheral length P, respectively.

The peripheral collector current can be rewritten as [REIN84]:

$$I_{CP} = \gamma_C \frac{P}{A} I_{CI} \tag{5.5}$$

where

$$\gamma_C \equiv \frac{C_P}{C_I} \exp\left(\frac{V_{RBI}}{V_T}\right). \tag{5.6}$$

V_{RBI} is the potential drop across R_{BI}, and γ_C is a function of bias and defines the current ratio at the emitter base junction. Dividing Eq. (5.1) by A and with the aid of Eq. (5.4), the total collector current density is:

$$J_C = J_{CI} + \gamma_C \frac{P}{A} J_{CI}. \tag{5.7}$$

Then from the J_C vs P/A plot for a fixed bias, γ_C is extracted using the least-square fitting [REIN84]. Collector spreading which might affect γ_C is accounted for independently in the intrinsic transistor model [JEON89].

The functional dependence of γ_C on collector current density as measured using the Rein approach above is given in Fig. 5.3. The fit to this data using the following equation

$$\gamma_C = a \left(\frac{I_{CI}}{A}\right)^b + c \tag{5.8}$$

has been incorporated into the model as shown in Fig. 5.3(a). Because of convergence problems in SLICE simulation, the functional form of γ_C has since been simplified to

$$\gamma_C = \gamma_{CO} + \alpha_C \left(\frac{I_{CI}}{A}\right) \tag{5.9}$$

and is shown in Fig. 5.3(b). This is used as an initial guess and is further fine-tuned by fitting the measured dc data as will be discussed later.

5.2.2 The Base Current Model

The base current comprises four components: back injection current into the emitter, the recombination current in the base-emitter junction space-charge-region, QNB, and in epitaxial collector region. Then the base current for one-dimensional charge-based BJT model can be expressed:

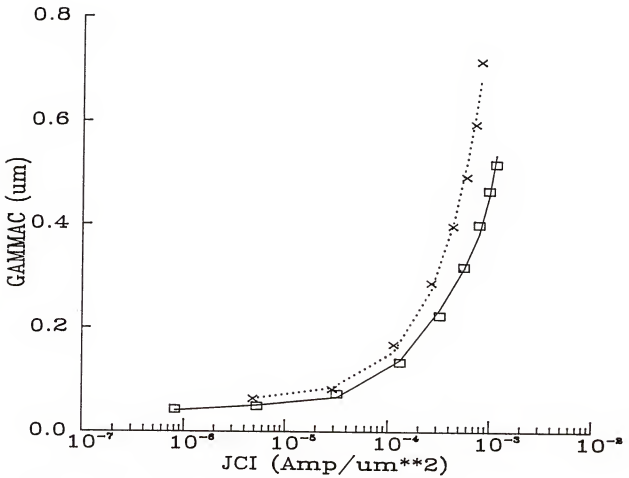


Fig. 5.3(a) The experimentally derived γ_C as a function of V_{BE} compared with simulation using Eq. (5.8). Note that γ_C is a function of V_{BC}. The data for γ_C for V_{BC} = 0V and for V_{BC} = -2V are shown by the □ and x, respectively, and the equivalent simulations by (____) and (···).

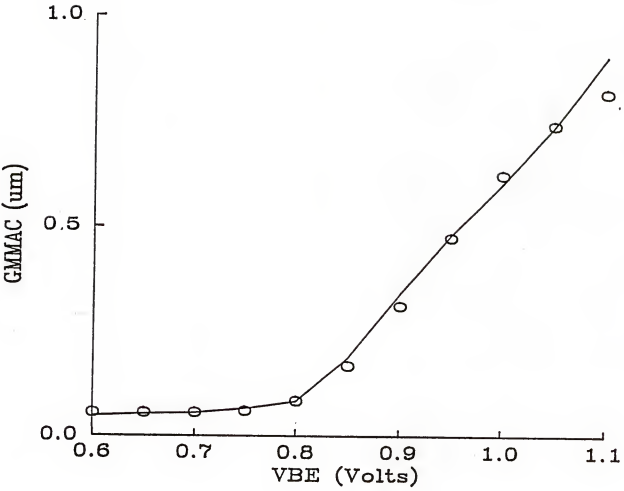


Fig. 5.3(b) The experimentally derived γ_C compared with simulation using Eq. (5.9). Although the data is taken for V_{BC} = -2V, We use the same fit for simulations at V_{BC} = 0V.

$$I_B = I_{EO}\left[\exp\left(\frac{V_{BE}}{V_T}\right) - 1\right] + I_{SEO}\left[\exp\left(\frac{V_{BE}}{n_{EB}V_T}\right) - 1\right] + \frac{Q_N}{\tau_B} + \frac{Q_{QNR}}{\tau_C} . \quad (5.10)$$

The intrinsic and peripheral base currents I_{BI} and I_{BP} are assumed to be predominantly emitter-recombination currents. The last two components of the base current in Eq. (5.10) [JEON89] are typically negligible in advanced BJT's except in low bias conditions. The base-emitter SCR recombination current is also negligible at intermediate and high current levels.

Then, the total base current is

$$I_B = I_{BI} + I_{BP}. \quad (5.11)$$

And the intrinsic and peripheral base currents can be expressed as:

$$I_{BI} = A\ B_I\left[\exp\left(\frac{V_{BE}}{V_T}\right) - \exp\left(\frac{V_{BCO}}{V_T}\right)\right] \quad (5.12)$$

$$I_{BP} = P\ B_P\left[\exp\left(\frac{V_{BEP}}{V_T}\right) - \exp\left(\frac{V_{BCOP}}{V_T}\right)\right] \quad (5.13)$$

respectively, where

$$\frac{B_P}{B_I} = \frac{J_{EOP}}{J_{EOI}}\ W_{EP} . \quad (5.14)$$

J_{EOI} and J_{EOP} are the emitter recombination current densities at zero bias. Using the Rein approach, the peripheral base current is:

$$I_{BP} = \gamma_B \frac{P}{A} I_{BI} . \tag{5.15}$$

It is assumed that γ_B is not a function of bias. This is a rough approximation and its value is fixed during the simulation of the dc and ac data [REIN87].

5.2.3 Charging Current Model

1. The Charges in the Quasi-Neutral Emitter Q_{EEI}, Q_{EEP}

In general, the hole charges stored in the emitter can be represented as:

$$Q_{EEI} = \tau_E I_{BI} \tag{5.16}$$

$$Q_{EEP} = \tau_{EP} I_{BP} \tag{5.17}$$

where τ_E is the emitter time constant which governs the hole transport and recombination in the monocrystalline emitter and polysilicon contact and we assume $\tau_E = \tau_{EP}$. τ_E is constant

because low injection conditions prevail in the heavily doped emitter. Some values for τ_E which can be used for an initial guess are given in [YUNG88] for polysilicon contacted emitters with and without interfacial layers. (In this reference, the quasi-static emitter delay τ_e for the majority carriers has to be multiplied by the current gain β to get τ_E here.) It has no effect on the dc simulations but its extraction is important for the small-signal model and will be discussed later.

The final relationship used in our model to simplify the number of charges is:

$$Q_{EEP} = \gamma_B \frac{P}{A} Q_{EEI} . \tag{5.18}$$

In the SLICE simulation, Q_{EEI} is calculated first in one-dimensional intrinsic transistor model, and Q_{EEP} is calculated using the relation in Eq. (5.18).

2. The Charges in the Quasi-Neutral Base Q_{BBI}, Q_{BBP}

The hole charge Q_{BB} in QNB (which is evaluated by Eqs.(2.11) in Section 2.3), for one-dimensional charge-based

model,can be expressed in terms of electron charge and ionized dopant charge based on quasi-neutrality [JEON89]:

$$Q_{BB} = qA \int_{y_E}^{y_C} n \, dx + qA \int_{y_E}^{y_C} N_A \, dx$$

$$\equiv Q_N + [Q_{JE} - Q_{JC}] + qAN_G \tag{5.19}$$

where N_G is the Gummel number and Q_{JE} and Q_{JC} will be defined in Eqs. (5.23)-(5.25).

The total hole charges in the intrinsic QNB, and extrinsic QNB can be:

$$Q_{BBI} = Q_{NI} + Q_{JEI} - Q_{JCI} \tag{5.20}$$

$$Q_{BBP} = Q_{NP} + Q_{JEP} - Q_{JCP} \tag{5.21}$$

where Q_{NI} and Q_{NP} are the electron charges for intrinsic region and peripheral region respectively.

Using Eqs. (2.11) and (5.5), the final simplifying relationship between intrinsic and peripheral hole charge in QNB is:

$$Q_{BBP} = \gamma_C \frac{P}{A} \frac{\overline{D_{NP}}}{D_{NI}} \exp\left(\frac{V_{RBI}}{V_T}\right) Q_{BBI} \tag{5.22}$$

where the ratio of the diffusivities may be used as a fitting parameter.

3. The Junction Capacitance Charges Q_{JEI}, Q_{JEP}, Q_{JCI}, Q_{JCP}

Unlike the previous treatment for one-dimensional model [JEON89], these charges are derived from ac measurements of the junction capacitances. As explained in Chapter 4, the emitter-base and base collector junction capacitances are separated into intrinsic and peripheral region junction capacitances as follows

$$C_{JI} = C_{JOI} A \left[1 + \frac{|V|}{\phi}\right]^m \tag{5.23}$$

$$C_{JP} = \left[C_{JOP} P + 4C_{CNR}\right] \left[1 + \frac{|V|}{\phi}\right]^m . \tag{5.24}$$

The ionized junction charges Q_{JI} and Q_{JP} are calculated using

$$Q_J = \int_0^V C_J \, dV . \tag{5.25}$$

The peripheral base-collector junction capacitance is further separated between the peripheral transistor and the extrinsic p^+/n junction by assuming a fixed ratio for the extrinsic to peripheral region. This ratio may be taken to be ~4 after Rein [REIN87]; or this ratio could be a fitting parameter; or the extrinsic region capacitance may be obtained from the slope of |Y12| as a junction of frequency [WIJN88].

4. The Charges in High Injection Q_{SCRI}, Q_{SCRP}, Q_{QNRI}, Q_{QNRP}

The ratio of the peripheral to intrinsic charges (Q_{SCRI}, Q_{SCRP}, Q_{QNRI}, Q_{QNRP}) in high injection is taken to be the ratio of the peripheral to intrinsic collector currents in high injection.

5. The Partitioned Base and Collector Charges Q_{BEI}, Q_{BEP}, Q_{BCI}, Q_{BCP}

The electron charge in QNB (Q_N) in (5.19) and the excess electron charge Q_{QNR} in the epitaxial collector (extended base) are shared between the emitter and collector terminals [JEON89]:

$$Q_{BE} = Q_{EE} + Q_N f_B + Q_{JE} + Q_{QNR} f_C \qquad (5.26)$$

$$Q_{BC} = Q_N (1 - f_B) + Q_{JC} + Q_{QNR} (1 - f_C) \quad (5.27)$$

where f_B and f_C are the charge partition factors which account for non-quasi-static effects in one-dimension (vertical) and are between 0 and 1. Q_{BEI}, Q_{BEP}, Q_{BCI}, and Q_{BCP} are defined as the same way as above. The small-signal response is not extremely sensitive to the specific value of f_B and f_C for the transistors under investigation [FOSS87].

5.2.4 Resistances

1. The Intrinsic Base Resistance R_{BI}

The model for intrinsic base resistance is an extension of Hauser's model for emitter crowding. It includes the high injection effects and base push-out implemented in the intrinsic transistor model and the details are given in Chapter 3.

2. The Parasitic Resistances R_{BX}, R_E, R_C

It is assumed that these resistances are independent of applied bias, but they are scalable. They are measured using the techniques in [GETR78] with the aid of J. S. Park and A. Neugroschel [PARK89] or Motorola information [MOTO88]. R_C does not include the epitaxial resistance in the collector

region. The epitaxial collector resistance is included in the currents and charges in the intrinsic transistor model [JEON89]. The complete multi-regional charge-based BJT model input parameters are explained in Table 5.1, 5.2, and 5.3.

5.3. Multi-Regional Charge-Based Small-Signal Model

There are two approaches for developing a small-signal model. One approach is to develop a small-signal model which stands alone from any large-signal model [WHIT70, KRON75]. This small-signal model is made by arranging the linearized elements that represent a distributed, geometrical structure and then extracting the appropriate parameters. An optimization program is used to fit the data for a given bias. This approach is inconvenient for simulating circuits with many different-sized transistors operating at varying bias conditions. Because this model is not derived from the large-signal model, it is not a general bias-dependant small-signal model. Therefore, the second more general and physical approach for modelling small-signal behavior [REIN87] is used. In this approach, the small-signal model elements are directly reduced from the large-signal model for a given bias.

When SLICE simulates the large-signal charge-based model, for each current source in the model, the derivatives

TABLE 5.1
TRANSISTOR SIZE-INDEPENDANT PARAMETERS

NAME	DESCRIPTION	UNITS
NAO	Extrapolated peak doping density at emitter-side QNB at equilibrium	Cm^{-3}
WBM	Metallurgical base width	Cm
η	Base doping gradient factor	-
WEPI	Epitaxial collector thickness	Cm
NEPI	Epitaxial doping density	Cm^{-3}
WSEO	Base-emitter equilibrium SCR width in base	Cm
PE	Base-emitter junction potential	V
ME	Base-emitter junction exponential factor	-
WSCO	Base-collector equilibrium SCR width in base	Cm
PC	Base-collector junction potential	V
MC	Base-collector junction exponential factor	-
DNI	Effective electron diffusivity in intrinsic base	$Cm^2\ s^{-1}$
DNP	Effective electron diffusivity in extrinsic base	$Cm^2\ s^{-1}$
γ_{CO}	Collector current separation coefficient at low bias	μm
α_C	Bias dependant collector current separation coefficient	-
γ_B	Base current separation coefficient	μm
JEO	Emitter saturation current density in intrinsic region	A/Cm^2

NAME	DESCRIPTION	UNITS
JSEO	Base-emitter SCR saturation current density in intrinsic region	A/Cm^2
n_{EB}	Base-emitter SCR emission coefficient	-
τ_E	Emitter hole transit time	s
τ_B	Carrier lifetime in base	s
τ_C	Carrier lifetime in collector	s
CF	Forward current coupling coefficient	-
CR	Reverse current coupling coefficient	-
FB	Base-charge partition factor	-
FC	Collector-charge partition factor	-

TABLE 5.2
JUNCTION CAPACITANCE PARAMETERS

NAME	DESCRIPTION	UNITS
CJEOI	Intrinsic base-emitter junction capacitance per unit area	$fF/\mu m^2$
CJEOP	Extrinsic base-emitter junction capacitance per unit length	$fF/\mu m$
CJCOI	Intrinsic base-collector junction capacitance per unit area	$fF/\mu m^2$
CJCOP	Extrinsic base-collector junction capacitance per unit length	$fF/\mu m$
ϕ_E	Base-emitter junction potential	V
m_E	Base-emitter junction exponential factor	-
ϕ_C	Base-collector junction potential	V
m_C	Base-collector junction exponential factor	-
CJECNR	One corner base-emitter junction capacitance	fF
CJCCNR	One corner base-collector junction capacitance	fF
CCS	Collector substrate junction capacitance	fF

TABLE 5.3
TRANSISTOR SIZE-DEPENDANT PARAMETERS

NAME	DESCRIPTION	UNITS
RE	Extrinsic emitter resistance	Ω
RBX	Extrinsic base resistance	Ω
RC	Extrinsic collector resistance	Ω
LE	Emitter window length (actual size)	μm
WE	Emitter window width (actual size)	μm

about the current-source control voltages are generated for a given bias. By rearranging these derivatives, we can derive a small-signal model which is composed of linearized elements.

For example, in the charge-based large-signal model (Fig. 5.1), I_{BI} is a function of the two independent voltages V_{BE} and V_{BC}. The corresponding small-signal current source i_{bi} can be expressed as

$$i_{bi} = \frac{\partial I_{bi}}{\partial V_{be}} v_{be} + \frac{\partial I_{bi}}{\partial V_{bc}} v_{bc} \quad . \tag{5.28}$$

This small-signal current source is composed of two different current sources which are controlled by the small-signal independent V_{be} and V_{bc}. The method to rearrange small-signal current source elements and derive linearized small-signal elements using this method, is shown in Fig. 5.4. Using this method, all large-signal current sources are rearranged into the linearized small-signal model elements as shown in Table 5.1. After all current sources are processed, the complete small-signal equivalent circuit is obtained which is shown in Fig. 5.5.

When the multi-regional charge-based small-signal model is derived, the transcapacitance element emerges as a new small-signal element. Unfortunately, there is not a

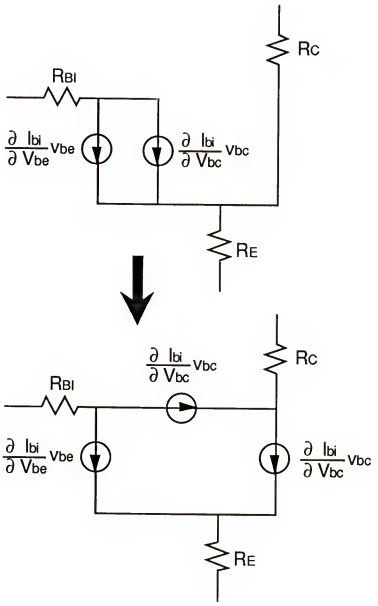


Fig. 5.4(a) Among the two component of Eq. (5.28) the small-signal current source $\frac{\partial I_{bi}}{\partial V_{bc}} v_{bc}$ is bridged across the collector side node.

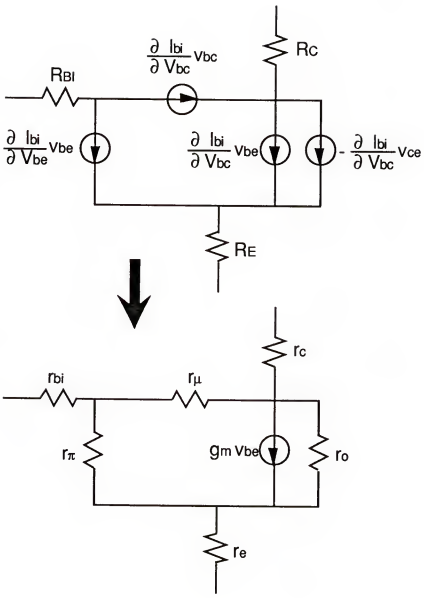


Fig. 5.4(b) With $v_{bc} = v_{be} - v_{ce}$, $\frac{\partial I_{bi}}{\partial v_{bc}} v_{bc}$ is divided into two current sources and all small-signal current sources are changed into the linearized elements.

TABLE 5.4
MULTI-REGIONAL SMALL-SIGNAL MODEL CIRCUIT ELEMENTS

CONDUCTANCES

$g_{\pi i} = \frac{\partial I_{BI}}{\partial V_{BE}}$	$g_{\pi p} = \frac{\partial I_{BP}}{\partial V_{BEP}}$
$g_{\mu i} = \frac{\partial I_{BI}}{\partial V_{BC}}$	$g_{\mu p} = \frac{\partial I_{BP}}{\partial V_{BCP}}$
$g_o = -\frac{\partial I_C}{\partial V_{BC}} - \frac{\partial I_{BI}}{\partial V_{BC}} - \frac{\partial I_{BP}}{\partial V_{BCP}}$	

CAPACITANCES

$C_{\pi i} = \frac{\partial Q_{BEI}}{\partial V_{BE}} + \frac{\partial Q_{BCI}}{\partial V_{BE}}$	$C_{\pi p} = \frac{\partial Q_{BEP}}{\partial V_{BEP}} + \frac{\partial Q_{BCP}}{\partial V_{BEP}}$
$C_{\mu i} = \frac{\partial Q_{BEI}}{\partial V_{BC}} + \frac{\partial Q_{BCI}}{\partial V_{BC}}$	$C_{\mu p} = \frac{\partial Q_{BEP}}{\partial V_{BCP}} + \frac{\partial Q_{BCP}}{\partial V_{BCP}}$
$C_o = \frac{\partial Q_{BEI}}{\partial V_{BC}} + \frac{\partial Q_{BEP}}{\partial V_{BCP}} - \frac{\partial Q_{SCR}}{\partial V_{BC}} - \frac{\partial Q_{SCRP}}{\partial V_{BCP}}$	$C_{bcx} = \frac{\partial Q_{BCX}}{\partial V_{BCX}}$

TRANSADMITTANCES

$y_{mi} = g_{mi} + j\omega\, b_{mi}$	$y_{mp} = g_{mp} + j\omega\, b_{mp}$
$g_{mi} = \frac{\partial I_C}{\partial V_{BE}} + \frac{\partial I_{BI}}{\partial V_{BC}} + \frac{\partial I_{BP}}{\partial V_{BCP}}$	$g_{mp} = \frac{\partial I_{BP}}{\partial V_{BCP}}$
$b_{mi} = \frac{\partial Q_{BEI}}{\partial V_{BC}} - \frac{\partial Q_{BCI}}{\partial V_{BE}} + \frac{\partial Q_{SCR}}{\partial V_{BE}} + \frac{\partial Q_{SCR}}{\partial V_{BC}}$	$b_{mp} = \frac{\partial Q_{BEP}}{\partial V_{BCP}} - \frac{\partial Q_{BCP}}{\partial V_{BEP}} + \frac{\partial Q_{SCRP}}{\partial V_{BEP}} + \frac{\partial Q_{SCRP}}{\partial V_{BCP}}$

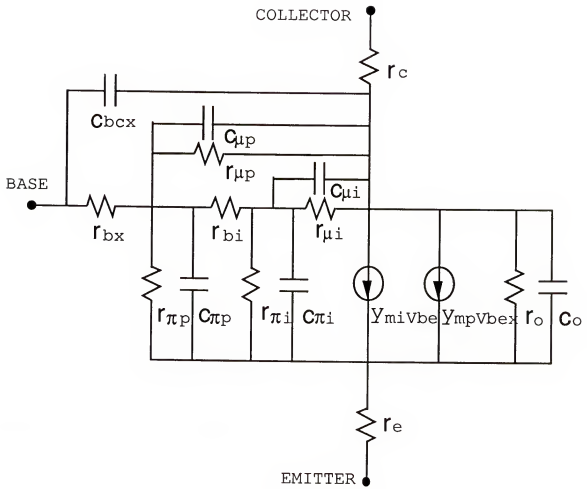


Fig. 5.5 The network representation of the multi-regional charge-based small-signal model. Although elements appear similar to Gummel-Poon (SPICE2) elements, their magnitude and physical origins are very different. Their relationship to the charges and currents of the large-signal model are given in Table 5.1. The transadmittances y_{mi} and y_{mp} are complex numbers.

transcapacitance circuit element available in SLICE. So a small-signal circuit simulator (SMACS) has been developed, which can simulate transcapacitance. The SMACS is written in FORTRAN, and can simulate circuit with up to 50 linearized elements for frequencies up to 100 GHz. It also has features to generate h-, y-, z- and s-parameters. The SMACS program source code is shown in Appendix B.

The small-signal equivalent circuit model which is taken from the derivatives of the charges and currents in the large-signal model is given in Fig. 5.3 and the derived small signal elements are given in Table 5.4. The small-signal elements have been derived after considerable rearrangement of the derivatives between the different parts as discussed in [MULL77] and in [FOSS87]. The charges and currents depend on the independent variables V_{BE}, V_{BEP}, V_{BC}, and V_{BCP}, and the derivatives of these terms are changed into capacitances, resistances, transcapacitances and transconductances. The transcapacitances appear in the imaginary parts of the transadmittances y_{mi} and y_{mp}. The multi-regional small-signal model has intrinsic and peripheral region components and p^+/n junction capacitance C_{BCX} as explained in Fig. 5.3.

5.4 Summary

The complete multi-regional charge-based large-signal model is developed. The collector and base currents are separated between the intrinsic transistor and peripheral transistor currents using an empirical technique. The collector separation constant is modelled as a function of applied emitter-base bias. The charging currents in the multi-regional small-signal model are modelled in a similar way. To account for the non-quasi-static effects, electron charges in quasi-nuetral base and the excess electron charges in the epitaxial collector are partitioned using charge partition factors. The junction capacitances are separated as described in the Chapter 4. The ionized junction charges are obtained by integrating the equivalent junction capacitances. The intrinsic base resistance (see Chapter 3) and the parasitic resistances are included in the complete the multi-regional charge-based large-signal model. The small-signal charge-based small-signal model is derived from the multi-regional model. The SMACS program is developed to simulate the multi-regional small-signal equivalent circuit which has transcapacitance elements which are not available in SLICE. The model input parameters and the small-signal circuit elements are given in table 5.4 and 6.1, respectively.

CHAPTER 6
DC AND AC MEASUREMENT AND VERIFICATION

6.1 INTRODUCTION

In previous chapter, a multi-regional charge-based small-signal model is developed. To verify this small-signal model, the multi-regional large-signal model is implemented in SLICE using UDCS and the extracted small-signal model elements for a given bias point are simulated in SMACS to generate h- and y-parameters. Dc and ac characteristics for the small-size high-speed self-aligned BJT's are measured and compared with simulated data in this chapter.

In Section 6.2, the dc measurements of three different emitter-size transistors are compared with the SLICE dc simulation data. For small-signal model verification, s-parameters are measured for these transistors, converted into h- and y-parameters, and compared with SMACS simulation results in Section 6.3. For most advanced self-aligned high-speed bipolar transistors, the cut-off frequency is higher than 1 GHz. To extract the BJT model parameters for SPICE such as τ_F and to characterize ac response, it is necessary to use a network analyzer for s-parameter measurement. Since the s-parameter measurement are very important in BJT

characterization and model verification, the measurement and calibration technique will be discussed in Section 6.3.

6.2 DC Verification of Multi-Regional Large-Signal Model

Test devices were fabricated at Motorola, Inc., using the MOSAIC III [ZDEB87] process (the third-generation Motorola Oxide Isolation Self-Aligned Implanted Circuits process). The test devices have self-aligned polysilicon contacts to the emitter and base with a boot-shaped sidewall spacer ~ 0.4 μm^2 in between. The drawn emitter areas vary from 1 X 4 μm^2 up to 2 X 12 μm^2. Data for γ_C, γ_B, C_{JC} and C_{JE} have been collected from all these devices (see Fig. 5.3 and Chapter 4) but the more extensive verification of the large- and small-signal charge-based models is only presented for three of these devices which have the correct layout for s-parameter measurements.

In Fig. 6.1(a), 6.1(b), and 6.1(c), SLICE simulation data and the dc measurement data for three transistors of different emitter dimensions 0.7 X 3.2 μm^2, 0.95 X 3.2μm^2, and 0.95 X 7.2 μm^2, respectively, are compared. V_{CE} vs I_C for I_B from 10 μA to 40 μA, Gummel Plot (I_C and I_B vs V_{BE} for V_{BC} = 0 V), and beta for V_{BC} = 0 and -2 V are compared. Their intrinsic base resistances as a function of V_{BE} for V_{BC} = 0 and -2 V are shown in Fig. 6.1(d). These transistors are

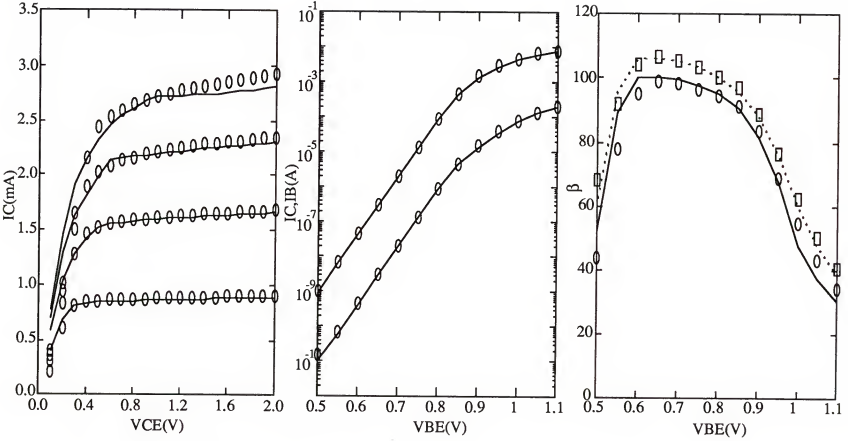


Fig. 6.1(a) Simulations of 0.7 X 3.2 μm2 emitter-size transistor using the multi-regional large-signal model and dc measurement data are compared; V_{CE} vs I_C for I_B from 10 μA to 40 μA, Gummel plot (V_{BC} = 0 V), and beta for V_{BC} = 0 (_____,o) and -2 V(....,□). Simulations are lines and measurement data are symbols (o,□).

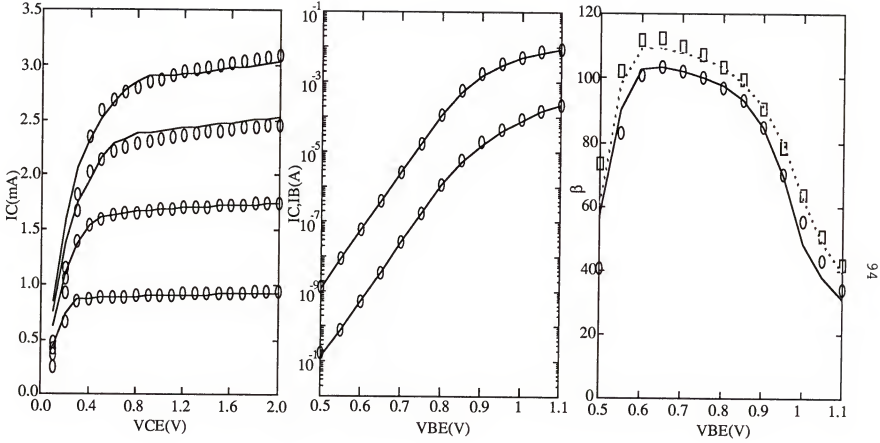


Fig. 6.1(b) Simulations of 0.95 X 3.2 μm2 emitter-size transistor using the multi-regional large-signal model and dc measurement data are compared; V_{CE} vs I_C for I_B from 10 μA to 40 μA, Gummel plot (V_{BC} = 0 V), and beta for V_{BC} = 0 (_____,o) and -2 V(....,□). Simulations are lines and measurement data are symbols (o,□).

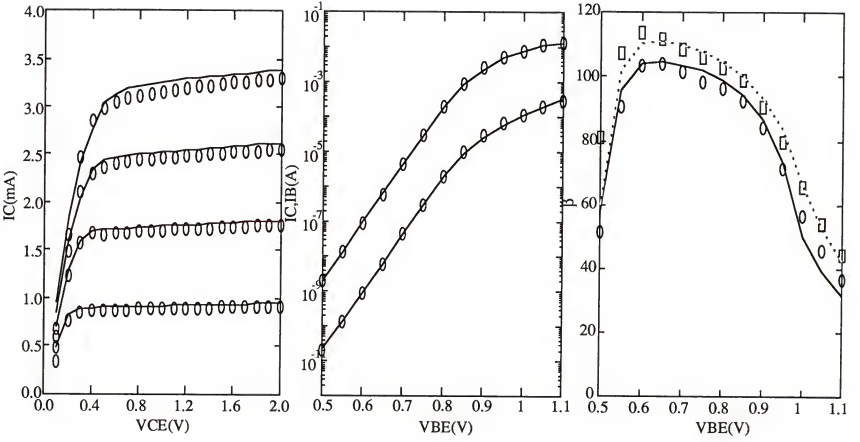


Fig. 6.1(c) Simulations of 0.95 X 7.2 μm2 emitter-size transistor using the multi-regional large-signal model and dc measurement data are compared; V_{CE} vs I_C for I_B from 10 μA to 40 μA, Gummel plot (V_{BC} = 0 V), and beta for V_{BC} = 0 (_____,o) and -2 V(....,□). Simulations are lines and measurement data are symbols (o,□).

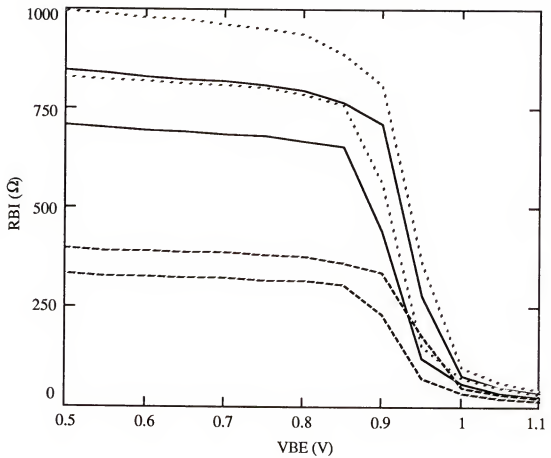


Fig. 6.1(d) The simulated R_{BI} for these transistors in Fig. 6.2(a) (_____), 6.1(b) (-----), and 6.1(c) (·····) at V_{BC} = OV (the lower R_{BI} plot for each set) and at V_{BC} = -2V.

later used in the s-parameter measurements. The experimental data was taken using an HP 4145 semiconductor parameter analyzer with the parameter extraction software (TECAP). The simulations include the relationship I_C, I_B, vs V_{BE}, I_C vs. V_{CE}, and β vs V_{BE} using the multi-regional large-signal model. All the model input parameters are given in Table 6.1. The profile information for these transistors is taken from the presentation given in [ZDEB87]. All the parasitic resistances and junction capacitances have been determined by independent measurements taken on each device using the conventional method [GETR78]. The definitions of the intrinsic transistor parameters are taken from [JEON89].

The goodness of the fits between the simulated and experimental data in Fig. 6.1 exemplifies the accuracy of the multi-regional model for varying transistor size and in high-current operation. These fits were obtained simultaneously for all three transistors. The input parameters which depend on the emitter area were the only parameters varied during the fitting process. These parameters are the emitter length L_E and width W_E and the parasitic emitter and collector resistance R_E and R_C.

At high currents, the simulation of β vs. V_{BE} at V_{BC} = 0 V is not as accurate as at V_{BC} = -2 V. We attribute this discrepancy to error in γ_C (V_{BE}). We use the γ_C taken from

TABLE 6.1
MULTI-REGIONAL MODEL INPUT PARAMETERS

N_{AO} = 8.0E17 cm^{-3}	W_{BM} = 1.24E-5 cm	η = 2.6
W_{EPI} = 0.375E-4 cm	N_{EPI} = 2.5E16 cm^{-3}	W_{SEO} = 1.5E-6 cm
P_E = 1.1	M_E = 0.4	W_{SCO} = 3.1E-6 cm
P_C = 0.75	M_C = 0.43	D_{NI} = 8.6 cm sec^{-1}
D_{NP} = 7.5 cm^2 sec^{-1}	W_{CI} = 0.22E-4 cm	γ_{CO} = 6.5E-2 μm
α_C = 20	γ_B = 0.127 μm	J_{EO} = 9.14E-13A/cm^2
J_{SEO} = 1.43E-8 A/cm^2	n_{EB} = 2.2	τ_B = 1.0E-6 sec
τ_C = 1.0E-5 sec	τ_E = 1.0E-9 sec	C_F = 0.5
C_R = 0.5	f_B = 0.5	f_C = 0.5
C_{JEOI} = 2.60 fF/μm^2	C_{JCOI} = 0.441 fF/μm^2	C_{JEOP} = 1.40 fF/μm
C_{JCOP} = 1.25 fF/μm	ϕ_E = 0.822 V	ϕ_C = 0.66 V
m_E = -0.34	m_C = -0.342	C_{JECNR} = 1.57 fF
C_{JCCNR} = 5.37 fF	C_{CS} = 54 fF	

Parameter	1.5X4 μm^2	1.75X4 μm^2	1.5x8 μm^2
L_E	3.2 μm	3.2 μm	7.2 μm
W_E	0.7 μm	0.95 μm	0.7 μm
R_E	18.5 Ω	16.5 Ω	11.2 Ω
R_{BX}	100 Ω	95 Ω	80 Ω
R_C	70 Ω	60 Ω	50 Ω

fits to the V_{BC} = -2 V data, but γ_C is also a function of V_{BC} as shown in Fig. 5.3(a). By more careful of fitting γ_C at V_{BC} = 0 V better dc fits can be obtained at this bias.

The magnitude of R_{BI} vs. V_{BE} reflects the scaling of the emitter window. For example, the R_{BI} for the emitter area 0.7 X 3.2 μm^2 is approximately double that for the emitter area 0.7 X 7.2 μm^2. Also, R_{BI} increases as the base width decreases with increasing V_{BC}.

6.3 S-Parameter Measurement and Calibration

High-frequency measurements (45 MHz - 26.5 GHz) were taken using an HP8510 Network Analyzer. Cascade Microwave probes were mounted on a Rucker and Kolls (model 1032) probe station which is grounded and the experiment was enclosed in a screen room. The s-parameter measurements were calibrated up to the probe tips using an Impedance Standard Substrate (ISS) made by Cascade Microtech, Inc. Then the embedded device-under-test (DUT) was measured and the y-parameters for the on-wafer open calibration pattern were subtracted from the embedded-device measurement [WIJN87]. This data is given in Fig. 6.2. The details of s-parameter calibration method is discussed in Appendix C. And in this chapter, the result is discussed.

The underlying assumption in de-embedding using the open

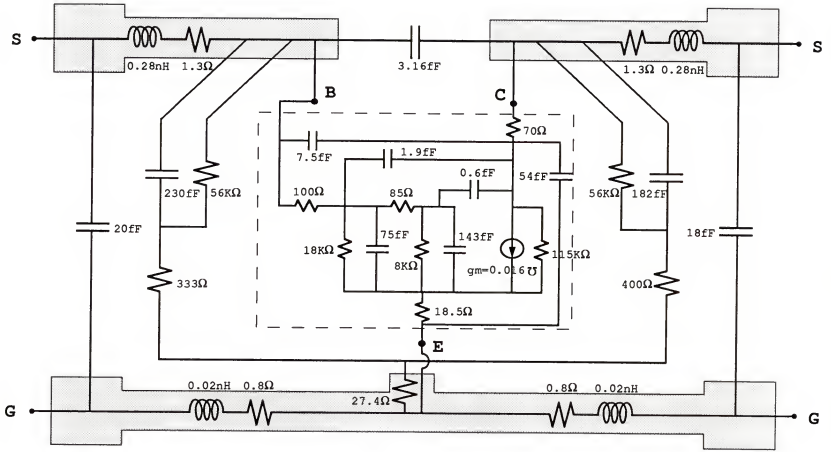


Fig. 6.2 The embedded small-signal equivalent model for a device (0.7 X 3.2 μm2) biased at its peak f_T (V_{BE} = 0.85V and V_{BC} = -2V). The small-signal transistor elements are reduced in size to set them apart from the embedding circuit elements.

on-wafer calibration technique is that the impedances associated with the pad and interconnect pattern in series with the DUT have negligible effect on the frequency response of the embedded device. To check the validity of this y-parameter subtraction method for our device and contact pad arrangement, we used MAESTRO [VAIT88] to find the equivalent de-embedding circuit. The complete circuit for the open, the short and the thru with the embedded device is given in Fig. 6.2. The small-signal elements for the 0.7 X 3.2 μm^2 device are given at the peak f_T biases, V_{BE} = 0.85 V and V_{BC} = -2 V. The series impedances (1.3 Ω + 0.28 nH and 0.8 Ω + 0.02 nH) inferred from the short and the thru are in fact insignificant compared to the terminal impedances of the DUT given in Fig. 6.2.

Although the measurement resolution of the HP 8510 is 0.001 dB, 0.01 degree and 0.01 ns [HEWL85], there can be large experimental error involved in the experimental design and the interpretation of the measurement. For example, the open on-wafer calibration pattern does not have the n/n^+ epitaxial layer which serves as collector and buried layer for the DUT. Therefore, there is possible error in de-embedding the DUT because the effect of the collector-to-substrate capacitance (given in Fig. 6.2) is not included in the measurement.For the simulation of the de-embedded data,

this capacitance is added to the output port of the small-signal model given in Fig.6.2. (This capacitance is treated as a lumped element when it probably should be distributed because of the significant difference in its area to that of the active device [ZDEB87].) In general, we attribute a ± 20% error in magnitude and a ± 6 degree error in phase of the h- and y-parameters at frequencies ≥ 1 GHz.

There is an inherent problem with the y-parameter subtraction technique when interpreting the output parameters of our bipolar transistor. As can be seen from Fig. 6.2, the capacitances associated with the embedding circuit are much larger than those at the device output port. The output y-parameters (y12 and y22) for the embedded-DUT have a small magnitude (10^{-4} to 10^{-5}) and these output parameters are of the same order of magnitude as the open-pattern output parameters (which are subtracted from them). Therefore, small errors arising from the interpretation of the measurements (such as de-embedding) will cause more error in the output parameters than in the input parameters.

It was difficult to obtain consistent data for our large (X 7.2 μm) devices when biased at V_{BC} = O V. s-parameter experimental technique is being improved so that more accurate measurements can be obtained in the future.

6.4 AC Verification of Multi-Regional Charge-Based Small-Signal Model

In Fig. 6.3, the SMACS simulations of the high-frequency experimental data (discussed in the previous section) are given for three different transistors 0.7 X 3.2 μm^2, 0.95 X 3.2μm^2, and 0.7 X 7.2 μm^2 in the common-emitter configuration. With no additional optimization except for r_{bi} (which will be described below), the simulations using the charge-based model are in relatively good agreement with the input-port h-parameters, h11 and h21, for all three transistors at the given bias conditions. Because of errors in our interpretation as discussed above, the agreement between the simulation and experimental data for the output port y-parameters, y12 and y22, is not as good (see discussion in Section 6.3). However, at the operating frequencies 1 GHz to f_T, the simulation shows similar trends to the phase and magnitude of the output parameters.

We use an ac value of r_{bi} which is smaller by a fitting factor < 1 from the dc value (as a function of bias as was shown in Fig. 6.1(d)). This factor is a parameter derived by fitting H21 as a function of frequency and bias. For the 0.95 X 3.2 μm^2 device, the ac value of r_{bi} thus defined is in agreement with the measured data given in the transistor data

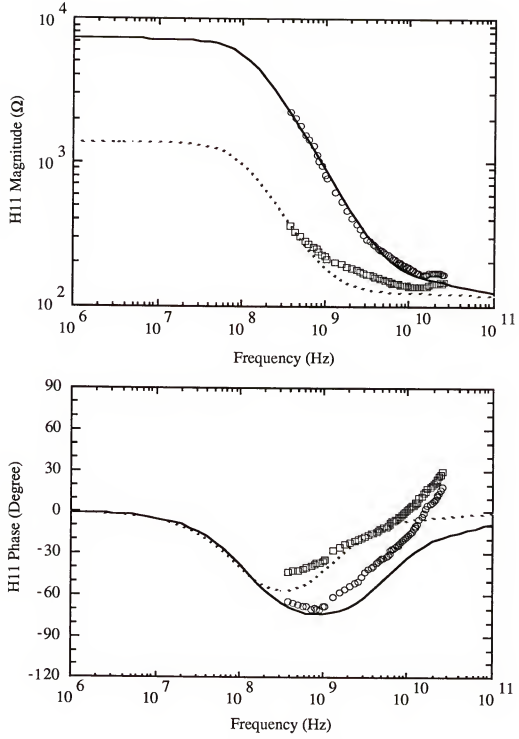


Fig. 6.3(a) Simulations (lines) and measurements (symbols) of the magnitude and phase of H11 for 0.7 X 3.2 μm2 emitter-size transistor, at V_{BE} = 0.85V (___, o) and V_{BE} = 0.95V (..., □) for V_{BC} = 0V.

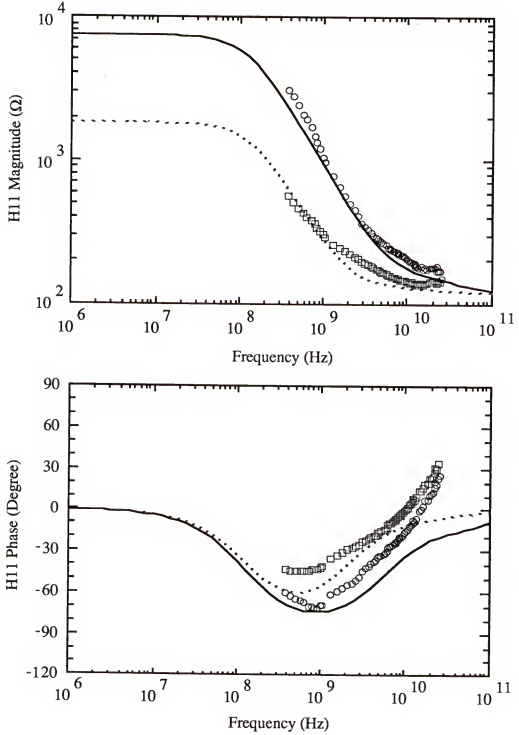


Fig. 6.3(b) Simulations (lines) and measurements (symbols) of the magnitude and phase of H11 for 0.7 X 3.2 μm2 emitter-size transistor, at V_{BE} = 0.85 V (___, o) and V_{BE} = 0.95V (..., □) for V_{BC} = -2V.

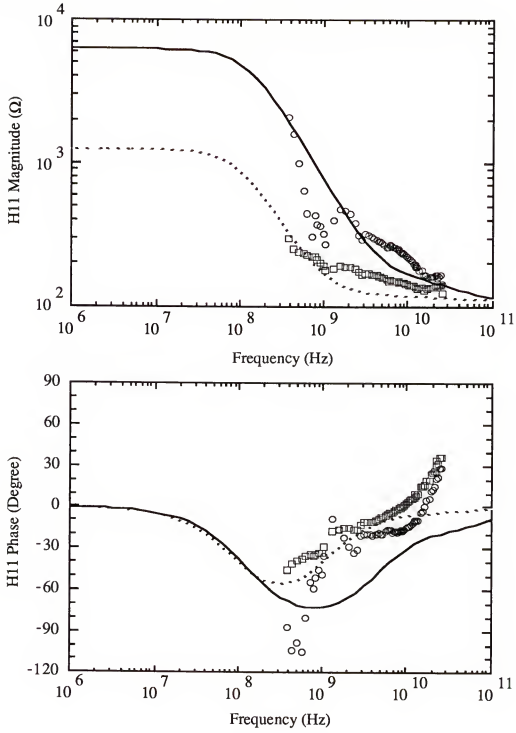


Fig. 6.3(c) Simulations (lines) and measurements (symbols) of the magnitude and phase of H11 for 0.95 X 3.2 μm2 emitter-size transistor, at V_{BE} = 0.85V (___, o) and V_{BE} = 0.95V (..., □) for V_{BC} = 0V.

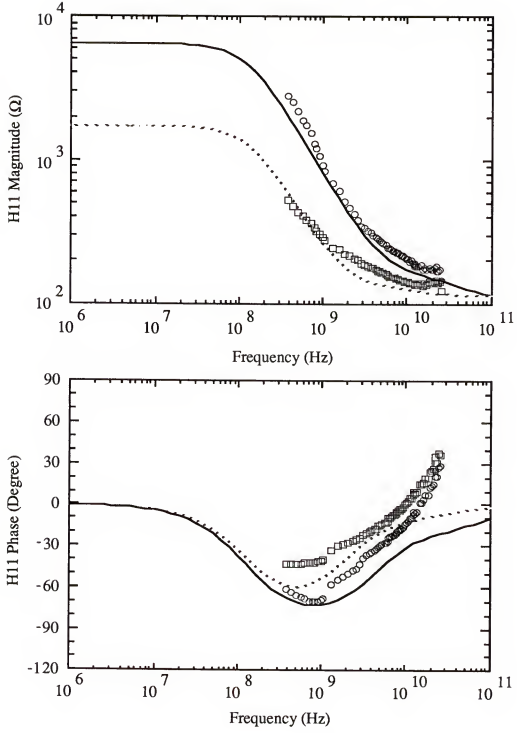


Fig. 6.3(d) Simulations (lines) and measurements (symbols) of the magnitude and phase of H11 for 0.95 X 3.2 μm2 emitter-size transistor, at V_{BE} = 0.85 V (___, o) and V_{BE} = 0.95V (..., □) for V_{BC} = -2V.

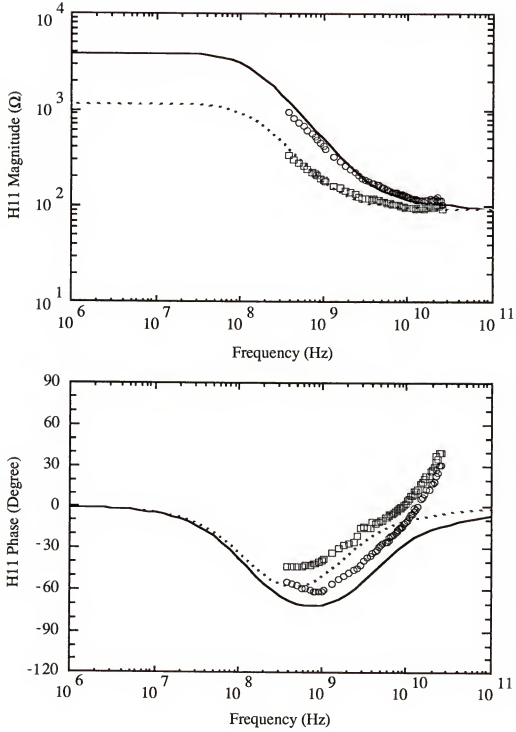


Fig. 6.3(e) Simulations (lines) and measurements (symbols) of the magnitude and phase of H11 for 0.7 X 7.2 μm2 emitter-size transistor, at V_{BE} = 0.85V (___, o) and V_{BE} = 0.95V (..., □) for V_{BC} = -2V.

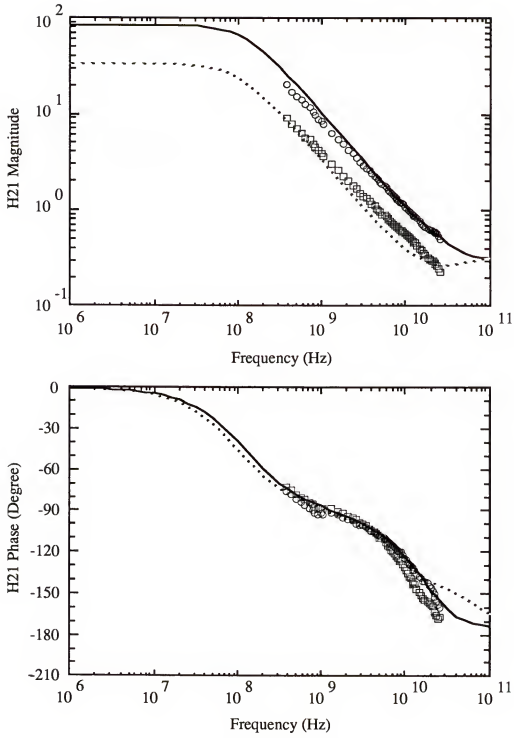


Fig. 6.3(f) Simulations (lines) and measurements (symbols) of the magnitude and phase of H21 for 0.7 X 3.2 μm2 emitter-size transistor, at V_{BE} = 0.85V (___, o) and V_{BE} = 0.95V (..., □) for V_{BC} = 0V.

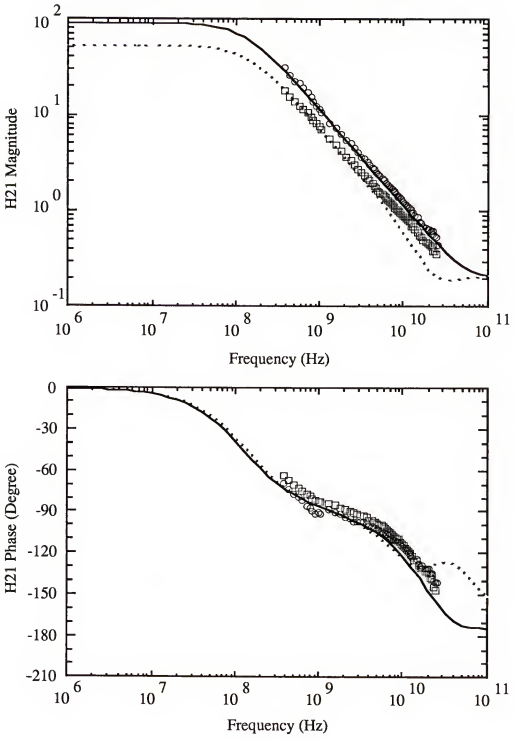


Fig. 6.3(g) Simulations (lines) and measurements (symbols) of the magnitude and phase of H21 for 0.7 X 3.2 μm2 emitter-size transistor, at V_{BE} = 0.85 V (___, o) and V_{BE} = 0.95V (..., ❑) for V_{BC} = -2V.

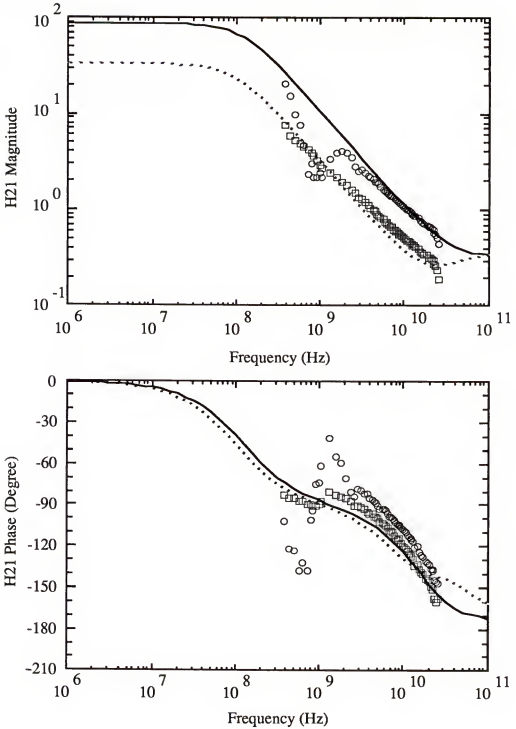


Fig. 6.3(h) Simulations (lines) and measurements (symbols) of the magnitude and phase of H21 for 0.95 X 3.2 μm2 emitter-size transistor, at V_{BE} = 0.85V (___, o) and V_{BE} = 0.95V (..., □) for V_{BC} = 0V.

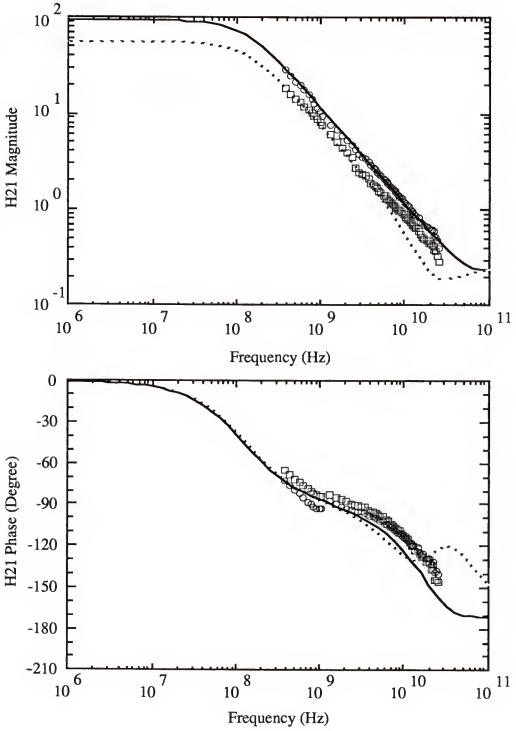


Fig. 6.3(i) Simulations (lines) and measurements (symbols) of the magnitude and phase of H21 for 0.95 X 3.2 μm2 emitter-size transistor, at V_{BE} = 0.85 V (___, o) and V_{BE} = 0.95V (..., □) for V_{BC} = -2V.

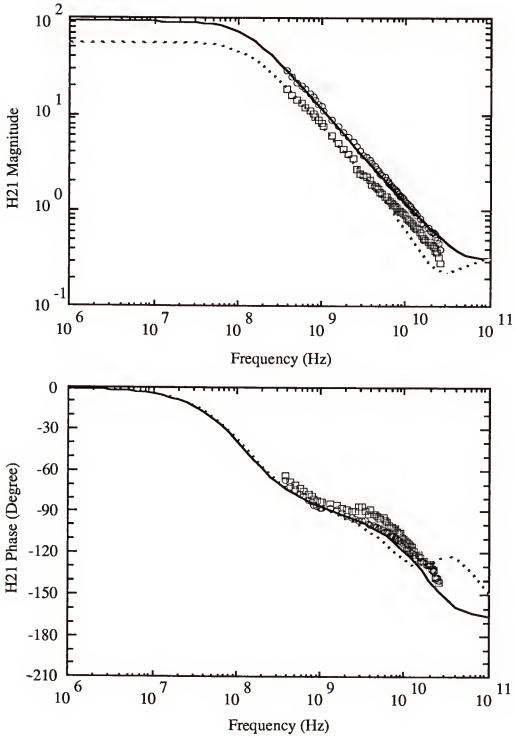


Fig. 6.3(j) Simulations (lines) and measurements (symbols) of the magnitude and phase of H21 for 0.7 X 7.2 μm2 emitter-size transistor, at V_{BE} = 0.85V (___, o) and V_{BE} = 0.95V (..., □) for V_{BC} = -2V.

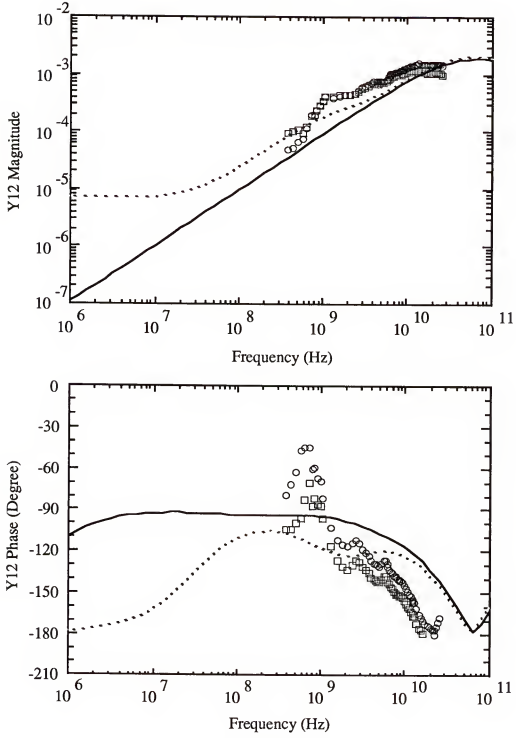


Fig. 6.3(k) Simulations (lines) and measurements (symbols) of the magnitude and phase of Y12 for 0.7 X 3.2 μm2 emitter-size transistor, at V_{BE} = 0.85V (___,o) and V_{BE} = 0.95V (...,□) for V_{BC} = 0V.

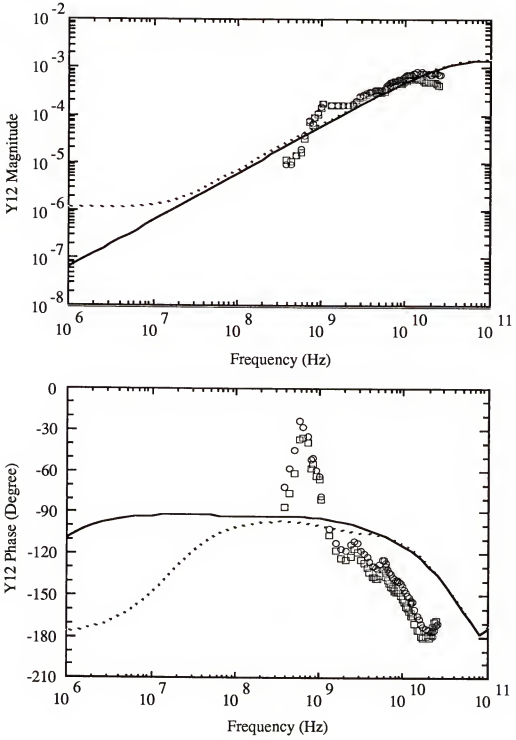


Fig. 6.3(1) Simulations (lines) and measurements (symbols) of the magnitude and phase of Y12 for 0.7 X 3.2 μm2 emitter-size transistor, at V_{BE} = 0.85 V (___, o) and V_{BE} = 0.95V (..., □) for V_{BC} = -2V.

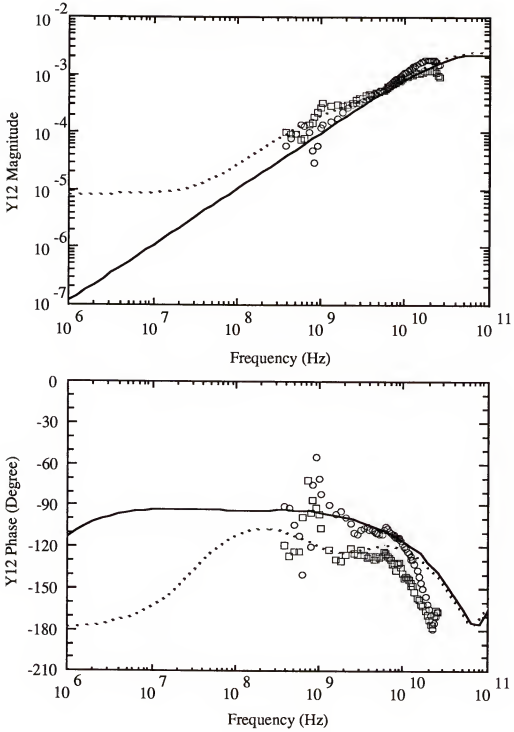


Fig. 6.3(m) Simulations (lines) and measurements (symbols) of the magnitude and phase of Y12 for 0.95 X 3.2 μm2 emitter-size transistor, at V_{BE} = 0.85V (___, o) and V_{BE} = 0.95V (..., □) for V_{BC} = 0V.

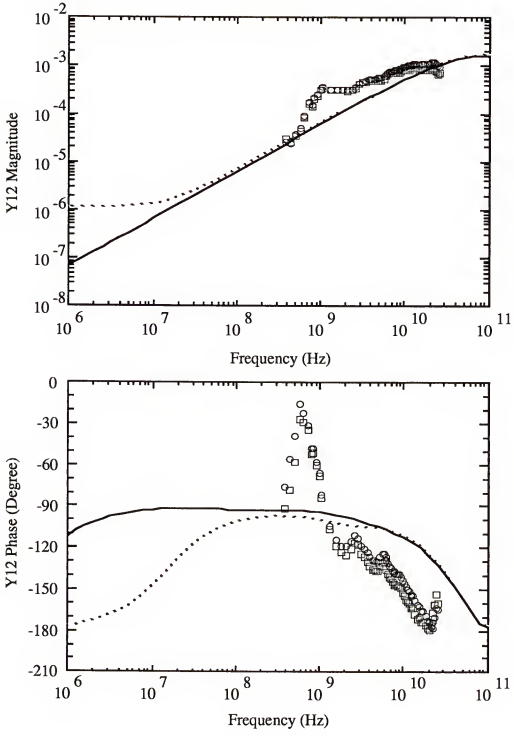


Fig. 6.3(n) Simulations (lines) and measurements (symbols) of the magnitude and phase of Y12 for 0.95 X 3.2 μm2 emitter-size transistor, at V_{BE} = 0.85 V (___, o) and V_{BE} = 0.95V (..., □) for V_{BC} = -2V.

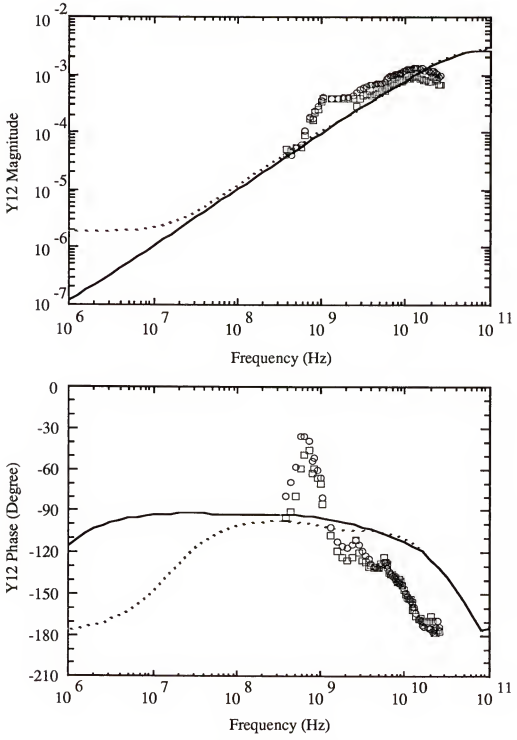


Fig. 6.3(o) Simulations (lines) and measurements (symbols) of the magnitude and phase of Y12 for 0.7 X 7.2 μm2 emitter-size transistor, at V_{BE} = 0.85V (___, o) and V_{BE} = 0.95V (..., □) for V_{BC} = -2V.

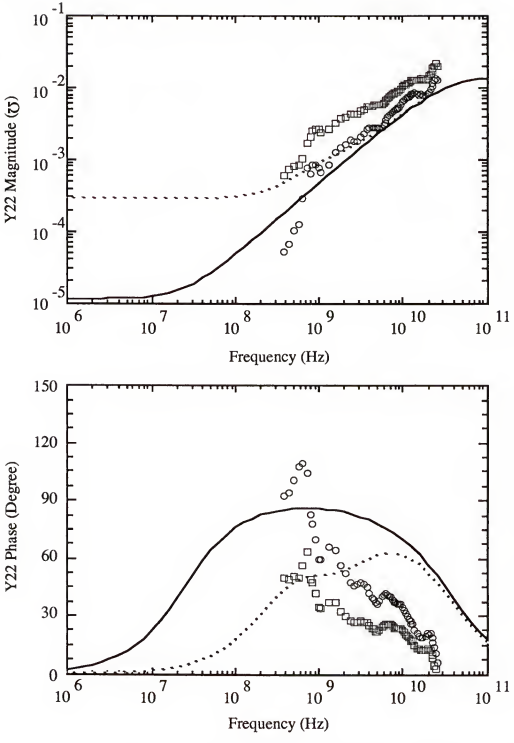


Fig. 6.3(p) Simulations (lines) and measurements (symbols) of the magnitude and phase of Y22 for 0.7 X 3.2 μm2 emitter-size transistor, at V_{BE} = 0.85V (___,o) and V_{BE} = 0.95V (...,❑) for V_{BC} = 0V.

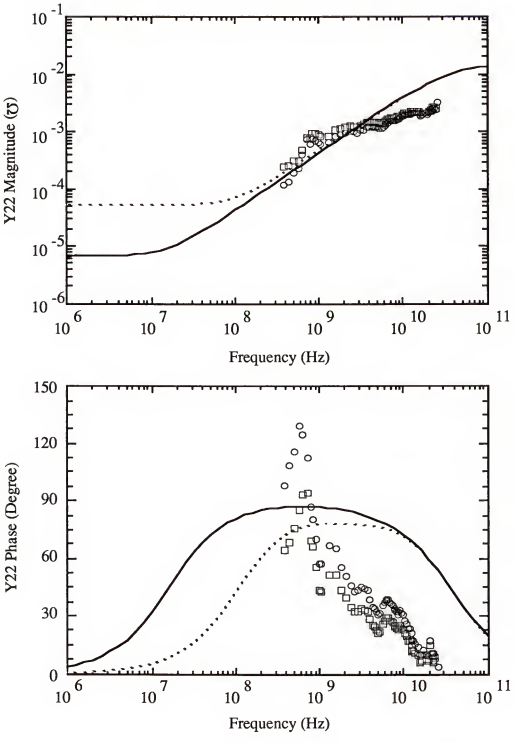


Fig. 6.3(q) Simulations (lines) and measurements (symbols) of the magnitude and phase of Y22 for 0.7 X 3.2 μm2 emitter-size transistor, at V_{BE} = 0.85 V (___, o) and V_{BE} = 0.95V (..., □) for V_{BC} = -2V.

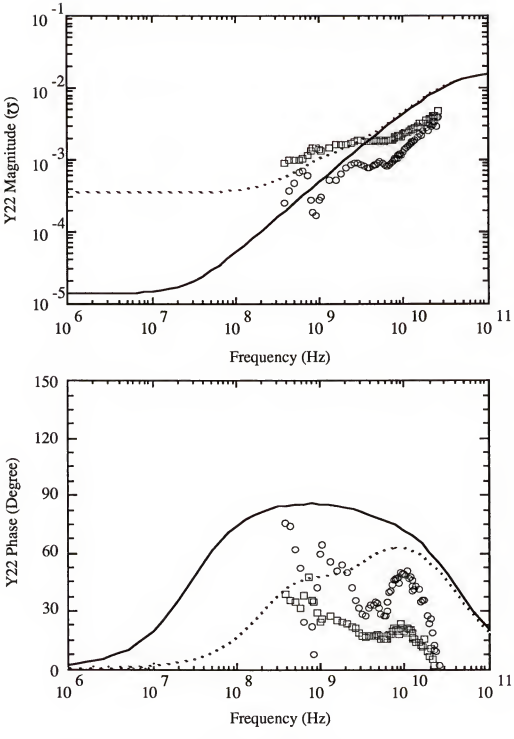


Fig. 6.3(r) Simulations (lines) and measurements (symbols) of the magnitude and phase of Y22 for 0.95 X 3.2 μm2 emitter-size transistor, at V_{BE} = 0.85V (___, o) and V_{BE} = 0.95V (..., □) for V_{BC} = 0V.

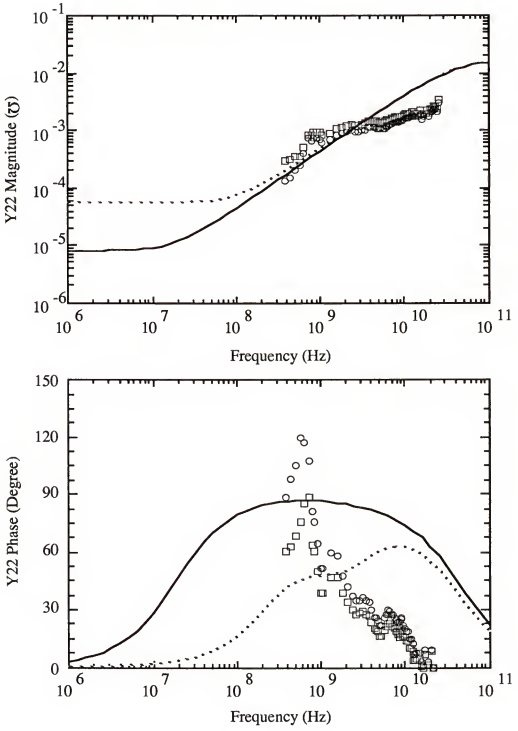


Fig. 6.3(s) Simulations (lines) and measurements (symbols) of the magnitude and phase of Y22 for 0.95 X 3.2 μm2 emitter-size transistor, at V_{BE} = 0.85 V (___,o) and V_{BE} = 0.95V (...,□) for V_{BC} = -2V.

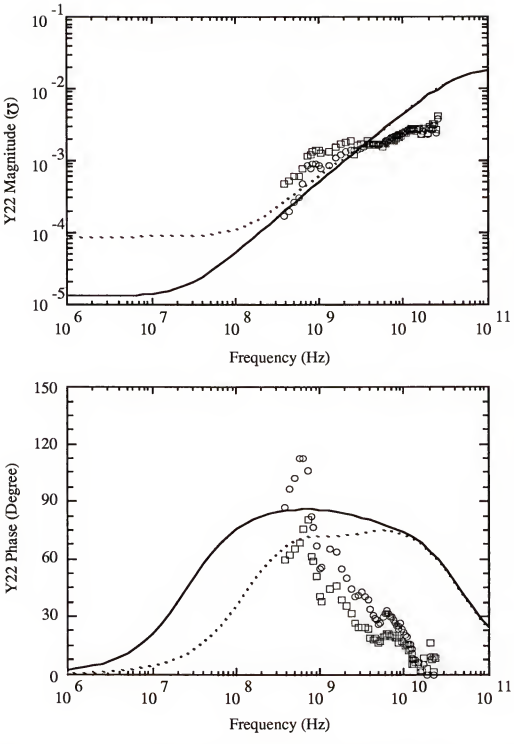


Fig. 6.3(t) Simulations (lines) and measurements (symbols) of the magnitude and phase of Y22 for 0.7 X 7.2 μm2 emitter-size transistor, at V_{BE} = 0.85V (___, o) and V_{BE} = 0.95V (..., □) for V_{BC} = -2V.

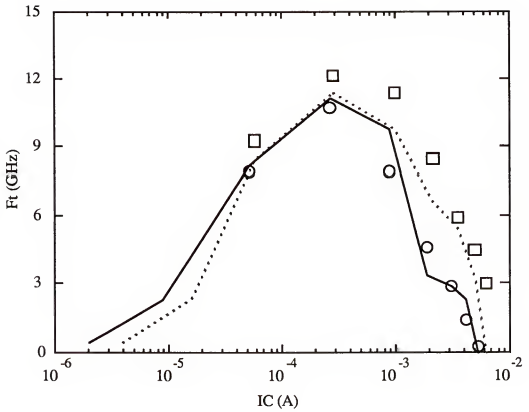


Fig. 6.4(a) Comparison of f_T vs I_C (V_{BE}) Simulation data with experimental data for 0.7 X 3.2 μm^2 emitter size transistor for V_{BC} = 0V (——,o) and V_{BC} = -2V (····,□).

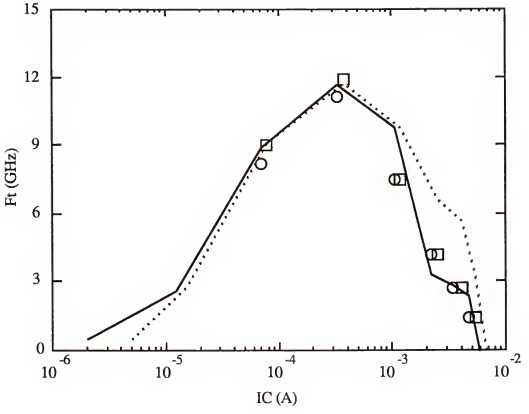


Fig. 6.4(b) Comparison of f_T vs I_C (V_{BE}) Simulation data with experimental data for 0.95 X 3.2 μm^2 emitter size transistor for V_{BC} = 0V (——,o) and V_{BC} = -2V (····,❑).

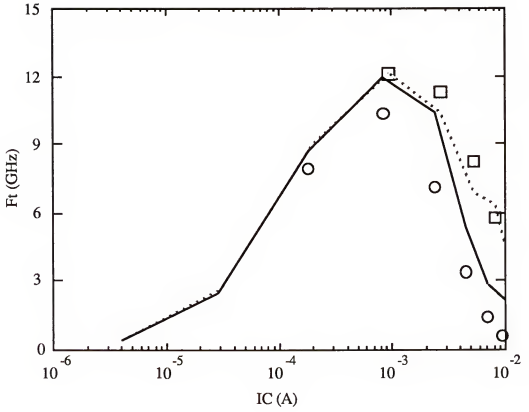


Fig. 6.4(c) Comparison of f_T vs I_C (V_{BE}) Simulation data with experimental data for 0.7 X 7.2 μm^2 emitter size transistor for V_{BC} = 0V (——,o) and V_{BC} = -2V (····,□).

book [MOTO88]. The variation of r_{bi} as a function of frequency has been reported by others [LARY85], [SCHM83] as being caused by the distributed nature of the base resistance which in the model is lumped.

In Fig. 6.4, simulated and experimental data for f_T vs. Ic(V_{BE}) are given. The measured values for f_T are taken at unity gain and not from the slope of the H21 magnitude as a function of frequency. The agreement between these data is good at peak values of f_T and within the error discussed in the last section. Although the overall shape of the simulated data is dependent on the model and its parameters (Table 6.4), the peak values in f_T are very sensitive to the emitter time constant τ_E. We use $\tau_E = 10^{-9}$ sec which is a value in agreement with our earlier predicted values of the emitter delay for the polysilicon-contacted emitters [YUNG88].

For small-signal circuits simulation, it is desirable to have a small-signal model with as few nodes as possible. Because the peripheral transistor is immediately adjacent to the intrinsic transistor and the peripheral-transistor base resistance is difficult to separate from the intrinsic-transistor base resistance, we re-arrange the peripheral small-signal elements $r_{\pi p}$, $c_{\pi p}$ and r_{bi} as in the inset of Fig.6.5. The simulation of the phase and magnitude H11 for the new configuration is compared in Fig. 6.5. Although there

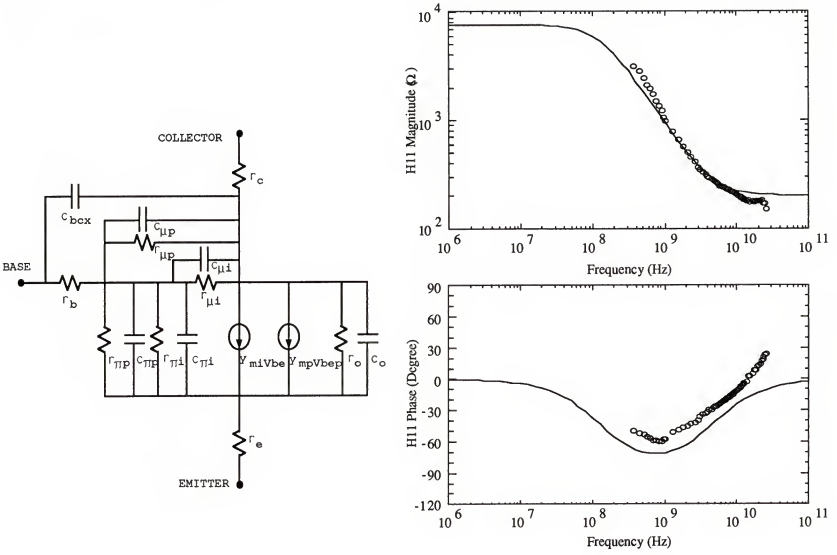


Fig. 6.5 Simulations of experimental data for the 0.7 X 3.2 μm2 device at V_{BE} = 0.85V and V_{BC} = -2V using the small-signal model configuration given in the inset.

is slightly better agreement in the phase and magnitude of H11, in equivalent simulations of H21, there is slightly worse agreement. By further optimizing the partition factors f_B and f_C, H21 can be fit better.

6.5 Summary

The multi-regional charge-based large-signal and small-signal models are partially verified using the advanced self-aligned high-speed bipolar transistors. For dc verification, V_{CE} vs I_C, the Gummel plot, and the dc current gain of the several different emitter-size transistors are compared with the SLICE UDCS simulation results. The large-signal model simulations agree within the experimental error with the dc measurements for varying bias and emitter size. s-parameter measurements are transformed to h- and y-parameters in order to verify the multi-regional charge-based small-signal model. The converted s-parameters are compared with the SMACS simulation for three different emitter-size transistors. The input port simulated data (h11 and h21) fits well the measured data for varying transistor size and in bias condition. However, the output port characteristics show discrepancies between the simulated and measured data. The errors in the output port measurement result from the collector buried layer capacitance which is different from

the open pattern buried layer and the experimental set-up. The s-parameter measurement and calibration methods are discussed in detail, but further verification is left for future work.

CHAPTER 7
CONCLUSION WITH RECOMMENDATIONS

A multi-regional charge-based small-signal BJT model is presented. This small-signal model is derived directly from a multi-regional change-based large-signal BJT model. The multi-regional large-signal model is based on the highly physical one-dimensional charge-based model, developed by H. Jeong and J. G. Fossum. The multi-regional model includes models for the intrinsic and peripheral (side-wall) transistor, the intrinsic base resistance linking the base regions of these two transistors and the base-collector extrinsic diode. Because of this regional approach, this model is scalable and more accurate for small-signal application than the one-dimensional model. For advanced bipolar technologies, the small-signal model can be derived directly from the large-signal model, i.e., no additional elements have to be added to account for the non-quasi-static effects. Non-quasi-static effects are modelled by partitioning the base charge between the emitter and collector sides and by subdividing the transistor into three regions.

The models for the three regions including the intrinsic base resistance use the output currents, charges and boundary conditions from the one-dimensional model in order to extend the one-dimensional model to include the peripheral transistor and the intrinsic base resistance. An approach suggested by Rein is used to link the peripheral transistor charges and currents directly to the intrinsic transistor. This approach is extended to include the high current region. Hauser's model for the intrinsic base resistance is expanded to include base push-out and conductivity modulation. An experimental technique is developed to separate the base-collector and emitter-base junction capacitances between the intrinsic, peripheral and extrinsic regions. This multi-regional large-signal model is implemented in UDCS in SLICE for CAD and has been verified with dc measurements over a large range of bias conditions and emitter size.

The small-signal model has some transcapacitance elements which are not available in SLICE. Therefore, a small-signal circuit simulator (SMACS) has been written for it. The other small-signal model elements are similar to those found in SPICE2 derived from a charge-control (Gummel-Poon) model, however their value may be different from a charge-based model. Partial verification of the small-signal model has been attempted for a large range of bias conditions

but a small variation in emitter geometry. s-parameter measurements, calibrated using open-pattern y-parameter subtraction method, have been interpreted with a knowledge of the interconnect and contact pad parasitics for the on-wafer open, through and short. Although this partial verification between the simulation and measurement has been confirmed for the common-emitter input port, the agreement between measurement and simulation is poor for the output port. A more accurate measurement of the output port is left for future work.

As future work, the following tasks are suggested to improve the model.

(1) For a more accurate model, the empirically linked intrinsic and peripheral transistor should be modeled more physically if possible and as a function of not only emitter-base voltage but also the base-collector voltage.

(2) For largest transistors, additional non-quasi-static effects have to be measured and modeled, and the new model then verified.

(3) To improve the computational efficiency, the multi-regional model needs to be simplified within the range of a certain accuracy.

(4) The multi-regional transistor model should be implemented into SPICE2 code for CAD application.

(5) The s-parameter measurement and calibration technique need to be refined for more accurate characterization of the high-speed BJTs.

(6) Scalable models for R_E, R_{BX}, R_C parameters have to be developed.

APPENIDIX A
JUNCTION CAPACITANCE SEPARATION PROGEAM (EXCAP)

```
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C                                                                     C
C     THIS PROGRAM IS TO SEPARATE JUNCTION CAPACTANCE                 C
C     USING THREE STEP METHOD WITHOUT CALIBRATION.                    C
C                                                                     C
C      TRANSISTOR DIMENSION INPUT FILE(CJ.D)                          C
C      Cje & Cjc MEASUREMENT INPUT FILE(CJE.M & CJC.M)                C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
      IMPLICIT REAL*12(A-H,O-Z)
      INTEGER Ibadtr(15)
      REAL*12 Cj(20,40),PERI(20),AREA(20),VBE(40)
      REAL*12 X(40),Y(40),SIG(40),A(6),LISTA(6),
     * COVAR(6,6),ALPHA(6,6)
      CHARACTER FILENM(50)*10
      COMMON/CONSTANT/SigmaA,SigmaP,Cje0i,Cje0p,Ntr,
     *Ifunction,Pie,Pme
      FILENM(15) = 'CJ.D'
      FILENM(16) = 'CJE.M'
      FILENM(17) = 'CJC.M'
      FILENM(18) = 'JUNK1'
      FILENM(19) = 'JUNK2'
      FILENM(20) = 'JUNK3'
      OPEN (UNIT=15, FILE = FILENM(15), STATUS = 'OLD')
      OPEN (UNIT=16, FILE = FILENM(16), STATUS = 'OLD')
      OPEN (UNIT=17, FILE = FILENM(17), STATUS = 'OLD')
      OPEN (UNIT=18, FILE = FILENM(18), STATUS = 'UNKNOWN')
      OPEN (UNIT=19, FILE = FILENM(19), STATUS = 'UNKNOWN')
      OPEN (UNIT=20, FILE = FILENM(20), STATUS = 'UNKNOWN')
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C                                                                     C
C READ DATA (CJM, AREA, P, V) & CHOOSE TR's TO USE                    C
C                                                                     C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
      Ifunction=1
      MA=4
      MFIT=4
      NCA=MA
      NOtr= 0
```

```
       READ (15,*)
      DO 10 L = 1,20
       NOtr = NOtr + 1
       READ (15,*, END=25) J, PERI(L), AREA(L)
10    CONTINUE
25    CONTINUE
       NOtr=NOtr-1
       NOvbe=23
      WRITE(3,*) 'Do you want to extract Cje0(1) or Cjc0(2)?'
      READ(3,*) Icj
        Icj=15+Icj
        READ(Icj,*)
      DO 155 Itr = 1, NOtr
        READ(Icj,*)
        READ(Icj,*)
      DO 255 Ivbe = 1, NOvbe
        READ(Icj,*) VBE(Ivbe), Cj(Itr,Ivbe)
        IF (VBE(Ivbe).EQ.0.) Ivbe0=Ivbe
        Y(Ivbe)=0.
255   CONTINUE
155   CONTINUE
      WRITE(3,*) 'Vbe range of optimization?'
       WRITE(3,*) 'Ivbe      Vbe'
      DO 277 Ivbe = 1, NOvbe
       WRITE(3,*) Ivbe,VBE(Ivbe)
277   CONTINUE
      WRITE(3,*) 'Vbe (start) in # ?'
      READ(3,*) Nstart
      WRITE(3,*) 'Vbe (stop) in # ?'
      READ(3,*) Nstop
      WRITE(3,*) 'Do you want to use all transistor?'
      WRITE(3,*) 'Yes(1) or No(2)?'
      READ(3,*) Ianswer
      IF(Ianswer.EQ.1) GO TO 355
      WRITE(3,*) 'How many transistors do not you want use?'
      READ(3,*) NObadtr
      DO 110 Ino = 1, NObadtr
      WRITE(3,*) 'Write the number of transistor which you
     * do not want use.'
       READ(3,*) Ibadtr(Ino)
110   CONTINUE
355   CONTINUE
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C                                                                     C
C STEP 1 >   THIS ROUTINE IS TO EXTRACT CJOI & CJOP                   C
C            USING LINEAR LEAST-SQUARE FIT                            C
C                                                                     C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
```

```
      SigmaX=0.
      SigmaY=0.
      SigmaXY=0.
      SigmaXX=0.
      PMAXX=0.
      NDATA=0
       DO 1550 Itr= 1, NOtr
          DO 1420 II= 1, NObadtr
            IF(Itr.EQ.Ibadtr(II)) GO TO 1550
1420       CONTINUE
       DO 1410 Jtr= Itr+1, NOtr
          DO 1520 II= 1, NObadtr
            IF(Jtr.EQ.Ibadtr(II)) GO TO 1410
1520       CONTINUE
      DELP=PERI(Itr)-PERI(Jtr)
      DELA=AREA(Itr)-AREA(Jtr)
      DELCJ=Cj(Itr,Ivbe0)-Cj(Jtr,Ivbe0)
        IF(DELA.EQ.0.)GO TO 1410
      SigmaX=SigmaX+DELP/DELA
      SigmaY=SigmaY+DELCJ/DELA
      SigmaXY=SigmaXY+DELP*DELCJ/DELA/DELA
      SigmaXX=SigmaXX+DELP*DELP/DELA/DELA
          NDATA=NDATA+1
       IF(PMAXX.LT.ABS(DELP/DELA)) PMAXX=ABS(DELP/DELA)
       WRITE(18,*)ABS(DELP/DELA),ABS(DELCJ*1.E15/DELA)
1410       CONTINUE
1550       CONTINUE
        Slope=(NDATA*SigmaXY-SigmaX*SigmaY)
     *         /(NDATA*SigmaXX-SigmaX*SigmaX)
        Cjeoi=(SigmaY-Slope*SigmaX)/NDATA
       WRITE(19,*) 0., Cjeoi*1.E15
       WRITE(19,*)10., (Cjeoi+Slope*10.)*1.E15
       WRITE(19,*)PMAXX, (Cjeoi+Slope*PMAXX)*1.E15
        Cjeop=Slope
        Cje0i=Cje0i
        Cje0p=Cje0p
      WRITE(3,*) 'Cje0i (in ff)=',Cjeoi
      WRITE(3,*) 'Cje0p (in ff)=',Cjeop
      WRITE(3,*) 'If you want to plot,stop here'
      read(3,*) dummy
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C                                                                     C
C STEP 2 >    THIS ROUTINE IS TO EXTRACT Pi & Me                      C
C             USING NON-LINEAR LEAST-SQUARE FIT                       C
C             (LEVENVERG-MARQUARDT METHOD)                            C
C                                                                     C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
      DO 800 IJK= 1,40
```

```
      SIG(IJK)=1.
      Y(IJK)=0
800   CONTINUE
      SigmaA=0.
      SigmaP=0.
       DO 550 Itr= 1, NOtr
          DO 420 II= 1, NObadtr
            IF(Itr.EQ.Ibadtr(II)) GO TO 550
420       CONTINUE
       DO 410 Jtr= Itr+1, NOtr
          DO 520 II= 1, NObadtr
            IF(Jtr.EQ.Ibadtr(II)) GO TO 410
520       CONTINUE
       NDATA=0
      IF ((Cj(Itr,Nstop)-Cj(Jtr,Nstop)).LT.0.) THEN
        SigmaA=SigmaA-(AREA(Itr)-AREA(Jtr))
        SigmaP=SigmaP-(PERI(Itr)-PERI(Jtr))
          DO 833 Ivbe= Nstop,Nstart,-1
          NDATA=NDATA+1
          X(NDATA)=VBE(Ivbe)
          Y(NDATA)=Y(NDATA)-(Cj(Itr,Ivbe)-Cj(Jtr,Ivbe))
833       CONTINUE
      ELSE
        SigmaA=SigmaA+(AREA(Itr)-AREA(Jtr))
        SigmaP=SigmaP+(PERI(Itr)-PERI(Jtr))
          DO 877 Ivbe= Nstop,Nstart,-1
          NDATA=NDATA+1
          X(NDATA)=VBE(Ivbe)
          Y(NDATA)=Y(NDATA)+(Cj(Itr,Ivbe)-Cj(Jtr,Ivbe))
877       CONTINUE
      ENDIF
410       CONTINUE
550       CONTINUE
CCCCCC  OPTIMIZE PARAMETER NUMBER  CCCCCCC
      LISTA(1)=1
      LISTA(2)=2
      LISTA(3)=3
      LISTA(4)=4
CCCCCC  INITIAL GUESS  CCCCCCC
        A(1)=Cje0i
      WRITE(3,*) ' Initial guess (Pie) ? '
      READ(3,*) A(2)
      WRITE(3,*) ' Initial guess (Me (<0.))? '
      READ(3,*) A(3)
        A(4)=Cje0p
CCCC  CHECK INITIAL  CHISQ CCCC
      ALAMDA=-1
      CALL MRQMIN(X,Y,SIG,NDATA,A,MA,LISTA,MFIT
```

```
     *         ,COVAR,ALPHA,NCA,CHISQ,ALAMDA)
      WRITE(3,*) ' Initial CHISQ =',CHISQ
CCCC  Main Loop  CCCCCCCCCCCCCC
      ICOUNT=0
      DO 300  ITER=1,500
         ICOUNT=ICOUNT+1
         CALL MRQMIN(X,Y,SIG,NDATA,A,MA,LISTA,MFIT
     *         ,COVAR,ALPHA,NCA,CHISQ,ALAMDA)
         WRITE(3,*) ITER, 'CHISQ =', CHISQ
         WRITE(3,*)  'A(1),A(2),A(3),A(4)'
         WRITE(3,*)   A(1),A(2),A(3),A(4)
         IF(ICOUNT.GT.20) THEN
            WRITE(3,*) ' Do you want stop? Yes(1),No(2)'
            READ(3,*) IANS
            IF(IANS.EQ.1) GO TO 400
            ICOUNT=0
         ENDIF
300   CONTINUE
400   ALAMDA=0.
      CALL MRQMIN(X,Y,SIG,NDATA,A,MA,LISTA,MFIT
     *         ,COVAR,ALPHA,NCA,CHISQ,ALAMDA)
      WRITE(3,*)' A(1) =  ', A(1)
      WRITE(3,*)' A(2) =  ', A(2)
      WRITE(3,*)' A(3) =  ', A(3)
      WRITE(3,*)' A(4) =  ', A(4)
      WRITE(3,*) 'Do you want to extract Ccorner?'
      WRITE(3,*) 'Yes(1) or No(2)?'
      READ(3,*) Ianswer
      IF(Ianswer.EQ.2) THEN
      DO 500 JJJ=1,NDATA
       XX=X(JJJ)
      YY=SigmaA*A(1)*(1.-X(JJJ)/A(2))**A(3)
     *  +SigmaP*A(4)*(1.-X(JJJ)/A(2))**A(3)
      WRITE(18,*) XX,YY
      WRITE(19,*) X(JJJ),Y(JJJ)
500   CONTINUE
      WRITE(20,*) 'A(1),A(2),A(3),A(4)'
      WRITE(20,*)  A(1)
      WRITE(20,*)  A(2)
      WRITE(20,*)  A(3)
      WRITE(20,*)  A(4)
       GO TO 955
      ENDIF
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C                                                                     C
C STEP 3 >   THIS ROUTINE IS TO EXTRACT Ccrn & Cprs                   C
C            USING NON-LINEAR LEAST-SQUARE FIT                        C
C            (LEVENVERG-MARQUARDT METHOD)                             C
```

```
C                                                                       C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
      WRITE(3,*) 'There are two method to choose.'
      WRITE(3,*) 'Method 1) optimise all 6 parameters
     *(Cji,Cjp, Ccorner,Pie,Me,Cparasitic).'
      WRITE(3,*) 'Method 2) optimise 2 parameters
     *(Ccorner,Cparasitsi).'
      WRITE(3,*) 'Method1(1) or Method2(2)?'
      READ(3,*)  IIanswer
        Cje0i=A(1)
        Pie=A(2)
        Pme=A(3)
        Cje0p=A(4)
      IF (IIanswer.EQ.1) THEN
        Ifunction=2
        MA=6
        MFIT=6
        NCA=MA
      ELSE
        Ifunction=3
        MA=2
        MFIT=2
        NCA=MA
      ENDIF
      DO 900 IJK= 1,40
      SIG(IJK)=1.
      Y(IJK)=0
900   CONTINUE
      SigmaA=0.
      SigmaP=0.
      Ntr=0
       DO 950 Itr= 1, NOtr
          DO 920 II= 1, NObadtr
            IF(Itr.EQ.Ibadtr(II)) GO TO 950
920       CONTINUE
       NDATA=0
       Ntr=Ntr+1
        SigmaA=SigmaA+AREA(Itr)
        SigmaP=SigmaP+PERI(Itr)
          DO 933 Ivbe= Nstop,Nstart,-1
          NDATA=NDATA+1
          X(NDATA)=VBE(Ivbe)
          Y(NDATA)=Y(NDATA)+Cj(Itr,Ivbe)
933       CONTINUE
950       CONTINUE
CCCCCC  OPTIMIZE PARAMETER NUMBER  CCCCCCC
      LISTA(1)=1
      LISTA(2)=2
```

```
      LISTA(3)=3
      LISTA(4)=4
      LISTA(5)=5
      LISTA(6)=6
CCCCCC  INITIAL GUESS  CCCCCCC
      IF (IIanswer.EQ.1) THEN
        A(1)=Cje0i
        A(2)=Cje0p
      WRITE(3,*) ' Initial guess(Ccorner (F))?'
      READ(3,*) A(3)
        A(4)=Pie
        A(5)=Pme
      WRITE(3,*) ' Initial guess(Cparasitic (F))?'
      READ(3,*) A(6)
      ELSE
      WRITE(3,*) ' Initial guess(Ccorner (F))?'
      READ(3,*) A(1)
      WRITE(3,*) ' Initial guess(Cparasitic (F))?'
      READ(3,*) A(2)
      ENDIF
CCCC  CHECK INITIAL  CHISQ CCCC
      ALAMDA=-1
      CALL MRQMIN(X,Y,SIG,NDATA,A,MA,LISTA,MFIT
     *          ,COVAR,ALPHA,NCA,CHISQ,ALAMDA)
      WRITE(3,*) ' Initial CHISQ =',CHISQ
CCCC  Main Loop  CCCCCCCCCCCCCC
      ICOUNT=0
      DO 911  ITER=1,500
         ICOUNT=ICOUNT+1
         CALL MRQMIN(X,Y,SIG,NDATA,A,MA,LISTA,MFIT
     *          ,COVAR,ALPHA,NCA,CHISQ,ALAMDA)
         WRITE(3,*) ITER, 'CHISQ =', CHISQ
         IF (IIanswer.EQ.1) THEN
         WRITE(3,*)  'A(1),A(2),A(3),A(4),A(5),A(6)'
         WRITE(3,*)   A(1),A(2),A(3),A(4),A(5),A(6)
         ELSE
         WRITE(3,*)  'A(1),A(2)'
         WRITE(3,*)   A(1),A(2)
         ENDIF
         IF(ICOUNT.GT.30) THEN
            WRITE(3,*) ' Do you want stop? Yes(1),No(2)'
            READ(3,*) IANS
            IF(IANS.EQ.1) GO TO 915
            ICOUNT=0
         ENDIF
911   CONTINUE
CCCCC Print out result CCCCCCCCC
915   ALAMDA=0.
```

```
      CALL MRQMIN(X,Y,SIG,NDATA,A,MA,LISTA,MFIT
     *          ,COVAR,ALPHA,NCA,CHISQ,ALAMDA)
       IF (IIanswer.EQ.1) THEN
          WRITE(3,*)' A(1) =  ', A(1)
          WRITE(3,*)' A(2) =  ', A(2)
          WRITE(3,*)' A(3) =  ', A(3)
          WRITE(3,*)' A(4) =  ', A(4)
          WRITE(3,*)' A(5) =  ', A(5)
          WRITE(3,*)' A(6) =  ', A(6)
          DO 916 JJJ=1,NDATA
            XX=X(JJJ)
            YY=(SigmaA*A(1)+SigmaP*A(2)+Ntr*A(3))
     *        *(1.-X(JJJ)/A(4))**A(5)+Ntr*A(6)
          WRITE(18,*) XX,YY
          WRITE(19,*) X(JJJ),Y(JJJ)
916       CONTINUE
          WRITE(20,*) 'A(1),A(2),A(3),A(4),A(5),A(6) '
          WRITE(20,*) 'Cje0i='
          WRITE(20,*)  A(1)
          WRITE(20,*) 'Cje0p='
          WRITE(20,*)  A(2)
          WRITE(20,*) 'Ccorner='
          WRITE(20,*)  A(3)
          WRITE(20,*) 'Pie='
          WRITE(20,*)  A(4)
          WRITE(20,*) 'Me='
          WRITE(20,*)  A(5)
          WRITE(20,*) 'Cpara.='
          WRITE(20,*)  A(6)
           DO 777 II= 1, NOtr
             CJT=A(1)*AREA(II)+A(2)*PERI(II)+A(3)
          WRITE(20,*) AREA(II),CJT
777        CONTINUE
       ELSE
          WRITE(3,*)' A(1) =  ', A(1)
          WRITE(3,*)' A(2) =  ', A(2)
          DO 316 JJJ=1,NDATA
            XX=X(JJJ)
            YY=(SigmaA*Cje0i+SigmaP*Cje0p+Ntr*A(1))
     *        *(1.-X(JJJ)/Pie)**Pme+Ntr*A(2)
          WRITE(18,*) XX,YY
          WRITE(19,*) X(JJJ),Y(JJJ)
316       CONTINUE
          WRITE(20,*) '       '
          WRITE(20,*) 'Cje0i='
          WRITE(20,*)  Cje0i
          WRITE(20,*) 'Cje0p='
          WRITE(20,*)  Cje0p
```

```
          WRITE(20,*) 'Ccorner='
          WRITE(20,*)  A(1)
          WRITE(20,*) 'Pie='
          WRITE(20,*)  Pie
          WRITE(20,*) 'Me='
          WRITE(20,*)  Pme
          WRITE(20,*) 'Cpara.='
          WRITE(20,*)  A(2)
           DO 377 II= 1, NOtr
             CJT=Cje0i*AREA(II)+Cje0p*PERI(II)+A(1)
          WRITE(20,*) AREA(II),CJT
377        CONTINUE
       ENDIF
955    CONTINUE
c
        CLOSE (15, STATUS = 'KEEP')
        CLOSE (16, STATUS = 'KEEP')
        CLOSE (17, STATUS = 'KEEP')
        CLOSE (18, STATUS = 'KEEP')
        CLOSE (19, STATUS = 'KEEP')
        CLOSE (20, STATUS = 'KEEP')
         stop
         end
       SUBROUTINE FUNCTION(X,A,Y,DYDA,NA)
       IMPLICIT REAL*12 (A-H,O-Z)
       REAL*12 A(NA),DYDA(NA)
       COMMON/CONSTANT/SigmaA,SigmaP,Cje0i,Cje0p,Ntr,
      * Ifunction,Pie,Pme
       IF (Ifunction.EQ.1) THEN
       Y=SigmaA*A(1)*(1.-X/A(2))**A(3)
      * +SigmaP*A(4)*(1.-X/A(2))**A(3)
       DYDA(1)=SigmaA*(1.-X/A(2))**A(3)
       DYDA(2)=(SigmaA*A(1)+SigmaP*A(4))*A(3)*
     *(1.-X/A(2))**(A(3)-1.)
     *        *X/A(2)/A(2)
       DYDA(3)=(SigmaA*A(1)+SigmaP*A(4))*QLOG(1.-X/A(2))
     *         *(1.-X/A(2))**A(3)
       DYDA(4)=SigmaP*(1.-X/A(2))**A(3)
       ELSE IF (Ifunction.EQ.2) THEN
       Y=(SigmaA*A(1)+SigmaP*A(2)+Ntr*A(3))
     *    *(1.-X/A(4))**A(5)+Ntr*A(6)
       DYDA(1)=SigmaA*(1.-X/A(4))**A(5)
       DYDA(2)=SigmaP*(1.-X/A(4))**A(5)
       DYDA(3)=Ntr*(1.-X/A(4))**A(5)
       DYDA(4)=(SigmaA*A(1)+SigmaP*A(2)+Ntr*A(3))*A(5)
     *        *(1.-X/A(4))**(A(5)-1.)*X/A(4)/A(4)
       DYDA(5)=(SigmaA*A(1)+SigmaP*A(2)+Ntr*A(3))
     *         *QLOG(1.-X/A(4))*(1.-X/A(4))**A(5)
```

```
      DYDA(6)=Ntr
      ELSE IF (Ifunction.EQ.3) THEN
      Y=(SigmaA*Cje0i+SigmaP*Cje0p+Ntr*A(1))
     *      *(1.-X/Pie)**Pme+Ntr*A(2)
      DYDA(1)=Ntr*(1.-X/Pie)**Pme
      DYDA(2)=Ntr
      ENDIF
      RETURN
      END
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C                                                                     C
C     SUBROUTINE: LEVENVERG-MARQUARDT METHOD                          C
C                                                                     C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
      SUBROUTINE MRQMIN(X,Y,SIG,NDATA,A,MA,LISTA,MFIT
     *          ,COVAR,ALPHA,NCA,CHISQ,ALAMDA)
      PARAMETER (MMAX=20)
      IMPLICIT REAL*12 (A-H,O-Z)
      REAL*12 X(NDATA),Y(NDATA),SIG(NDATA),A(MA),LISTA(MFIT),
     * COVAR(NCA,NCA),ALPHA(NCA,NCA),ATRY(MMAX),BETA(MMAX),
     * DA(MMAX),ONEDA(20,20)
      IF(ALAMDA.LT.0.)THEN
         KK=MFIT+1
         DO 12 J=1,MA
            IHIT=0
            DO 11 K=1,MFIT
               IF(LISTA(K).EQ.J)IHIT=IHIT+1
11          CONTINUE
            IF(IHIT.EQ.0) THEN
               LISTA(KK)=J
               KK=KK+1
            ELSE IF (IHIT.GT.1) THEN
               WRITE(3,*) 'Improper permutatiopn in LISTA'
            ENDIF
12       CONTINUE
         IF(KK.NE.(MA+1)) WRITE(3,*) 'Improper permutation in
     *LISTA'
         ALAMDA=.001
         CALL MRQCOF(X,Y,SIG,NDATA,A,MA,LISTA,MFIT,ALPHA,BETA
     *     ,NCA,CHISQ)
         OCHISQ=CHISQ
         DO 13 J=1,MA
            ATRY(J)=A(J)
13       CONTINUE
      ENDIF
      DO 15 J=1,MFIT
         DO 14 K=1,MFIT
            COVAR(J,K)=ALPHA(J,K)
```

```
14        CONTINUE
          COVAR(J,J)=ALPHA(J,J)*(1.+ALAMDA)
          ONEDA(J,1)=BETA(J)
15        CONTINUE
       CALL GAUSSJ(COVAR,MFIT,NCA,ONEDA,1,1)
       DO 30 J=1,MFIT
          DA(J)=ONEDA(J,1)
30     CONTINUE
       IF(ALAMDA.EQ.0.) THEN
          CALL COVSRT(COVAR,NCA,MA,LISTA,MFIT)
          RETURN
       ENDIF
       DO 16 J=1,MFIT
          ATRY(LISTA(J))=A(LISTA(J))+DA(J)
16     CONTINUE
       CALL MRQCOF(X,Y,SIG,NDATA,ATRY,MA,LISTA,MFIT,COVAR,DA
      *     ,NCA,CHISQ)
       IF(CHISQ.LT.OCHISQ) THEN
          ALAMDA=0.1*ALAMDA
          OCHISQ=CHISQ
          DO 18 J=1,MFIT
             DO 17 K=1,MFIT
                ALPHA(J,K)=COVAR(J,K)
17           CONTINUE
             BETA(J)=DA(J)
             A(LISTA(J))=ATRY(LISTA(J))
18        CONTINUE
       ELSE
          ALAMDA=10.0*ALAMDA
          CHISQ=OCHISQ
       ENDIF
       RETURN
       END
       SUBROUTINE MRQCOF(X,Y,SIG,NDATA,A,MA,LISTA,MFIT
      *          ,ALPHA,BETA,NALP,CHISQ)
       PARAMETER (MMAX=20)
       IMPLICIT REAL*12 (A-H,O-Z)
       REAL*12 X(NDATA),Y(NDATA),SIG(NDATA),ALPHA(NALP,NALP)
      *   ,BETA(MA),DYDA(MMAX),LISTA(MFIT)
       DO 12 J=1,MFIT
             DO 11 K=1,J
                ALPHA(J,K)=0.
11           CONTINUE
             BETA(J)=0.
12        CONTINUE
       CHISQ=0.
       DO 15 I=1,NDATA
          CALL FUNCTION(X(I),A,YMOD,DYDA,MA)
```

```
      SIG2I=1./(SIG(I)*SIG(I))
      DY=Y(I)-YMOD
      DO 14 J=1,MFIT
         WT=DYDA(LISTA(J))*SIG2I
         DO 13 K=1,J
            ALPHA(J,K)=ALPHA(J,K)+WT*DYDA(LISTA(K))
13       CONTINUE
         BETA(J)=BETA(J)+DY*WT
14    CONTINUE
      CHISQ=CHISQ+DY*DY*SIG2I
15    CONTINUE
      DO 17 J=2,MFIT
         DO 16 K=1,J-1
            ALPHA(K,J)=ALPHA(J,K)
16       CONTINUE
17    CONTINUE
      RETURN
      END
      SUBROUTINE GAUSSJ(A,N,NP,B,M,MP)
      PARAMETER(NMAX=50)
      IMPLICIT REAL*12 (A-H,O-Z)
      REAL*12 A(NP,NP),B(NP,MP),IPIV(NMAX),INDXR(NMAX),
     *INDXC(NMAX)
      DO 11 J=1,N
         IPIV(J)=0
11    CONTINUE
      DO 22 I=1,N
         BIG=0.
         DO 13 J=1,N
            IF(IPIV(J).NE.1) THEN
               DO 12 K=1,N
                  IF(IPIV(K).EQ.0) THEN
                     IF(ABS(A(J,K)).GE.BIG) THEN
                        BIG=ABS(A(J,K))
                        IROW=J
                        ICOL=K
                     ENDIF
                  ELSE IF(IPIV(K).GT.1) THEN
                     WRITE(3,*) 'Singular matrix'
                  ENDIF
12             CONTINUE
            ENDIF
13       CONTINUE
         IPIV(ICOL)=IPIV(ICOL)+1
         IF(IROW.NE.ICOL) THEN
            DO 14 L=1,N
               DUM=A(IROW,L)
               A(IROW,L)=A(ICOL,L)
```

```
                A(ICOL,L)=DUM
14            CONTINUE
              DO 15 L=1,M
                 DUM=B(IROW,L)
                 B(IROW,L)=B(ICOL,L)
                 B(ICOL,L)=DUM
15            CONTINUE
           ENDIF
           INDXR(I)=IROW
           INDXC(I)=ICOL
           IF(A(ICOL,ICOL).EQ.0.) WRITE(3,*) 'Singular matrix'
           PIVINV=1./A(ICOL,ICOL)
           A(ICOL,ICOL)=1.
           DO 16 L=1,N
              A(ICOL,L)=A(ICOL,L)*PIVINV
16         CONTINUE
           DO 17 L=1,M
              B(ICOL,L)=B(ICOL,L)*PIVINV
17         CONTINUE
           DO 21 LL=1,N
              IF(LL.NE.ICOL) THEN
                 DUM=A(LL,ICOL)
                 A(LL,ICOL)=0.
                 DO 18 L=1,N
                    A(LL,L)=A(LL,L)-A(ICOL,L)*DUM
18               CONTINUE
                 DO 19 L=1,M
                    B(LL,L)=B(LL,L)-B(ICOL,L)*DUM
19               CONTINUE
              ENDIF
21         CONTINUE
22      CONTINUE
        DO 24 L=N,1,-1
           IF(INDXR(L).NE.INDXC(L)) THEN
              DO 23 K=1,N
                 DUM=A(K,INDXR(L))
                 A(K,INDXR(L))=A(K,INDXC(L))
                 A(K,INDXC(L))=DUM
23            CONTINUE
           ENDIF
24      CONTINUE
        RETURN
        END
        SUBROUTINE  COVSRT(COVAR,NCVM,MA,LISTA,MFIT)
        IMPLICIT REAL*12 (A-H,O-Z)
        REAL*12 COVAR(NCVM,NCVM),LISTA(MFIT)
        DO 12 J=1,MA-1
           DO 11 I=J+1,MA
```

```
            COVAR(I,J)=0.
11          CONTINUE
12      CONTINUE
        DO 14 I=1,MFIT-1
           DO 13 J=I+1,MFIT
              IF(LISTA(J).GT.LISTA(I)) THEN
                 COVAR(LISTA(J),LISTA(I))=COVAR(I,J)
              ELSE
                 COVAR(LISTA(I),LISTA(J))=COVAR(I,J)
              ENDIF
13         CONTINUE
14      CONTINUE
        SWAP=COVAR(1,1)
        DO 15 J=1,MA
           COVAR(1,J)=COVAR(J,J)
           COVAR(J,J)=0.
15      CONTINUE
        COVAR(LISTA(1),LISTA(1))=SWAP
        DO 16 J=2,MFIT
           COVAR(LISTA(J),LISTA(J))=COVAR(1,J)
16      CONTINUE
        DO 18 J=2,MA
           DO 17 I=1,J-1
              COVAR(I,J)=COVAR(J,I)
17         CONTINUE
18      CONTINUE
        RETURN
        END
```

APPENIDIX B
SMALL-SIGNAL CIRCUIT SIMULATOR (SMACS)

```
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C                                                                     C
C     THIS PROGRAM IS TO SIMULATE SMALL-SIGNAL CIRCUIT                C
C     WITH LINEARIZED ELEMENTS USING GAUSS-ELIMINATION                C
C     METHOD AND TO GENERATE H-, Z-, Y- AND S-PARAMETERS.             C
C                                                                     C
C                 <Available circuit elements>                        C
C     R--- Resistance, C--- Capacitance, L--- Inductance              C
C     Y(Real)--- Transconductance,                                    C
C     Y(Imaginary)--- Transcapacitance                                C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
      IMPLICIT REAL*12 (A-B)
      INTEGER N1(2,30),N2(2,30),N3(2,30),N4(2,30),N
      INTEGER NH(2,30),NL(2,30),NMAX(2),NNH(2),NNL(2)
      INTEGER H11NODE(4),H22NODE(4)
      REAL*12 VALUE(2,30),HVALUE(4),RE(2,30),IM(2,30),W,F(51)
      REAL*12 C1,C2,XX,PI,YY
      COMPLEX  CH(4),CS11,CS12,CS21,CS22,CSN,CH21
      COMPLEX  H11,H12,H21,H22
      COMPLEX  Y11,Y12,Y21,Y22
      CHARACTER ELM(2,30)*1,EELM(2,30)*4,FILENM(30)*10
      CHARACTER*3 H11FRONT,H11REAR,H22FRONT,H22REAR
      COMMON /CC/ A(20,20,2),B(20,2)
      FILENM(10) = 'CKT'
* H-PARAMETERS FILE
      FILENM(11) = 'H11S-P'
      FILENM(12) = 'H21S-P'
      FILENM(13) = 'H12S-P'
      FILENM(14) = 'H22S-P'
* Y-PARAMETERS FILE
      FILENM(15) = 'Y11S-P'
      FILENM(16) = 'Y21S-P'
      FILENM(17) = 'Y12S-P'
      FILENM(18) = 'Y22S-P'
* S-PARAMETERS FILE
      FILENM(19) = 'S11S-C'
      FILENM(20) = 'S21S-C'
      FILENM(21) = 'S12S-C'
```

```
      FILENM(22) = 'S22S-C'
      PI= 4.0*ATAN(1.0)
      H11FRONT = 'RBB '
      H11REAR  = 'REE '
      H22FRONT = 'RBB '
      H22REAR  = 'REE '
      DO 9 I = 1,5
         J = (I-1)*10
         IF (I .EQ. 1) THEN
         T = 1E6
         ELSE IF (I .EQ. 2) THEN
         T = 1E7
         ELSE IF (I .EQ. 3) THEN
         T = 1E8
         ELSE IF (I .EQ. 4) THEN
         T = 1E9
         ELSE
         T = 1E10
         END IF
         F(J+1) = 1.000*T
         F(J+2) = 1.259*T
         F(J+3) = 1.585*T
         F(J+4) = 1.995*T
         F(J+5) = 2.512*T
         F(J+6) = 3.162*T
         F(J+7) = 3.981*T
         F(J+8) = 5.012*T
         F(J+9) = 6.310*T
         F(J+10) = 7.943*T
9     CONTINUE
      F(51) = 1.E11
      OPEN (UNIT=10, FILE = FILENM(10), STATUS = 'OLD')
      DO 14 M = 11, 22
            OPEN (UNIT=M, FILE = FILENM(M), STATUS =
     *           'UNKNOWN')
14    CONTINUE
CCC   CLEAR EVERY ARRAYS  CCC
      DO 11 I = 1,2
         NMAX(I) = 0
         NNH(I) = 0
         NNL(I) = 0
      DO 11 L = 1,30
         ELM(I,L) = ' '
         EELM(I,L) = '    '
         NH(I,L) = 0
         NL(I,L) = 0
         RE(I,L) = 0
         IM(I,L) = 0
```

```
         VALUE(I,L) = 0.0
11     CONTINUE
       DO 12 I = 1,30
          B(I,1) = 0.0
          B(I,2) = 0.0
       DO 12 J = 1,30
          A(I,J,1)= 0.0
          A(I,J,2)= 0.0
12     CONTINUE
       DO 13 I = 1,4
          H11NODE(I) = 0
          H22NODE(I) = 0
          HVALUE(I) = 0.0
13     CONTINUE
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C                                                                      C
C      READ SMALL-SIGNAL CIRCUIT FILE                                  C
C                                                                      C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
       I = 1
29     DO 20 L = 1,30
       READ (10,*, END=25)EELM(I,L),NH(I,L),NL(I,L),VALUE(I,L)
       ELM(I,L) = EELM(I,L)
         IF (I .EQ. 1) THEN
              IF (EELM(1,L) .EQ. H11FRONT)
                H11NODE(1) = NH(I,L)
                H11NODE(2) = NL(I,L)
                HVALUE(1) = VALUE(I,L)
              END IF
              IF (EELM(1,L) .EQ. H11REAR)
                H11NODE(3) = NH(I,L)
                H11NODE(4) = NL(I,L)
                HVALUE(2) = VALUE(I,L)
              END IF
        ELSE
              IF (EELM(2,L) .EQ. H22FRONT)
                H22NODE(1) = NH(I,L)
                H22NODE(2) = NL(I,L)
                HVALUE(3) = VALUE(I,L)
              END IF
              IF (EELM(2,L) .EQ. H22REAR)
                H22NODE(3) = NH(I,L)
                H22NODE(4) = NL(I,L)
                HVALUE(4) = VALUE(I,L)
              END IF
        END IF
           IF (ELM(I,L) .EQ. 'V   ')
                NNH(I) = NH(I,L)
```

```
            NNL(I) = NL(I,L)
          END IF
          IF ( NH(I,L) .GT. NMAX(I) ) NMAX(I) = NH(I,L)
          IF ( NL(I,L) .GT. NMAX(I) ) NMAX(I) = NL(I,L)
          IF (ELM(I,L) .EQ. 'Y   ') THEN
           READ (10,*) N1(I,L),N2(I,L),N3(I,L),N4(I,L)
     *      ,RE(I,L),IM(I,L)
              IF ( N1(I,L) .GT. NMAX(I) ) NMAX(I) = N1(I,L)
              IF ( N2(I,L) .GT. NMAX(I) ) NMAX(I) = N2(I,L)
              IF ( N3(I,L) .GT. NMAX(I) ) NMAX(I) = N3(I,L)
              IF ( N4(I,L) .GT. NMAX(I) ) NMAX(I) = N4(I,L)
          END IF
          IF (ELM(I,L) .EQ. 'N')
          I = 2
          GO TO 29
          END IF
20     CONTINUE
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C                                                                      C
C     MAIN DO LOOP TO CALCULATE H-PARAMETERS                           C
C                                                                      C
C DO-LOOP 40 ; FREQ CHANGE                                             C
C DO-LOOP 50 ; GENERATE H-PARAMETERS                                   C
C DO-LOOP 60 & 70 ; GENERATE ARRAY A( ) FOR SUBROUTINE                 C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
25     DO 111 K = 1,51
          W = 2 * PI * F(K)
        FREQ=F(K)
       DO 50 I = 1, 2
         DO 60 L = 1, 30
          IF ( ELM(I,L) .EQ. 'R' ) THEN
           XX =  1.0/VALUE(I,L)
           A(NH(I,L),NH(I,L),1) = A(NH(I,L),NH(I,L),1) + XX
           A(NH(I,L),NL(I,L),1) = A(NH(I,L),NL(I,L),1) - XX
           A(NL(I,L),NH(I,L),1) = A(NL(I,L),NH(I,L),1) - XX
           A(NL(I,L),NL(I,L),1) = A(NL(I,L),NL(I,L),1) + XX
          ELSE IF ( ELM(I,L) .EQ. 'L' ) THEN
           XX =  1.0/(W*VALUE(I,L))
           A(NH(I,L),NH(I,L),2) = A(NH(I,L),NH(I,L),2) - XX
           A(NH(I,L),NL(I,L),2) = A(NH(I,L),NL(I,L),2) + XX
           A(NL(I,L),NH(I,L),2) = A(NL(I,L),NH(I,L),2) + XX
           A(NL(I,L),NL(I,L),2) = A(NL(I,L),NL(I,L),2) - XX
          ELSE IF ( ELM(I,L) .EQ. 'C' ) THEN
           XX =  W*VALUE(I,L)
           A(NH(I,L),NH(I,L),2) = A(NH(I,L),NH(I,L),2) + XX
           A(NH(I,L),NL(I,L),2) = A(NH(I,L),NL(I,L),2) - XX
           A(NL(I,L),NH(I,L),2) = A(NL(I,L),NH(I,L),2) - XX
           A(NL(I,L),NL(I,L),2) = A(NL(I,L),NL(I,L),2) + XX
```

```
          ELSE IF ( ELM(I,L) .EQ. 'Y' ) THEN
           XX = W*IM(I,L)
           A(N3(I,L),N1(I,L),1)=A(N3(I,L),N1(I,L),1)+RE(I,L)
           A(N3(I,L),N1(I,L),2) = A(N3(I,L),N1(I,L),2)+XX
           A(N3(I,L),N2(I,L),1) = A(N3(I,L),N2(I,L),1)-
             RE(I,L)
           A(N3(I,L),N2(I,L),2) = A(N3(I,L),N2(I,L),2)-XX
           A(N4(I,L),N1(I,L),1) = A(N4(I,L),N1(I,L),1)-
             RE(I,L)
           A(N4(I,L),N1(I,L),2) = A(N4(I,L),N1(I,L),2)-XX
           A(N4(I,L),N2(I,L),1) = A(N4(I,L),N2(I,L),1)
             +RE(I,L)
           A(N4(I,L),N2(I,L),2) = A(N4(I,L),N2(I,L),2)+XX
          END IF
60        CONTINUE
          DO 70  LL = 1,NMAX(I)
           A(LL,NNL(I),1) = 0.0
           A(LL,NNL(I),2) = 0.0
           A(NNL(I),LL,1) = 0.0
           A(NNL(I),LL,2) = 0.0
70        CONTINUE
          A(NNL(I),NNH(I),1) = 1.0
          A(NNL(I),NNH(I),2) = 0.
          A(NNH(I),NNL(I),1) = 1.0
          A(NNH(I),NNL(I),2) = 0.
          B(NNL(I),1) = 1.0
          B(NNL(I),2) = 0.
          N = NMAX(I)
          DO 999 IJ=1,NMAX(I)
          C1 = A(NNL(I),IJ,1)
          C2 = A(NNL(I),IJ,2)
          A(NNL(I),IJ,1) = A(NNH(I),IJ,1)
          A(NNL(I),IJ,2) = A(NNH(I),IJ,2)
          A(NNH(I),IJ,1) = C1
          A(NNH(I),IJ,2) = C2
999       CONTINUE
          C1 = B(NNL(I),1)
          C2 = B(NNL(I),2)
          B(NNL(I),1) = B(NNH(I),1)
          B(NNL(I),2) = B(NNH(I),2)
          B(NNH(I),1) = C1
          B(NNH(I),2) = C2
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C                                                                      C
C      SOLVE ADMITTANCE MATRIX USING GAUSS-ELIMINATION                 C
C      METHOD AND GENERATE H-PARAMETERS                                C
C                                                                      C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
```

```
      CALL GE(N)
      IF (I .EQ. 1) THEN
*H11
      B(H11NODE(2),1) = (B(H11NODE(1),1) - B(H11NODE(2),1))
     */ HVALUE(1)
      B(H11NODE(2),2) = (B(H11NODE(1),2) - B(H11NODE(2),2))
     */ HVALUE(1)
      CALL DIVI(B(H11NODE(1),1),B(H11NODE(1),2),
     *B(H11NODE(2),1),B(H11NODE(2),2),C1,C2)
      CH(1) = CMPLX (C1,C2)
      H11 = CH(1)
         HM = CABS(H11)
         HP = 180.*2.*ATAN((HM-REAL(H11))/AIMAG(H11)) / PI
         WRITE (11,*) FREQ,HM,HP
      CH(1) = CH(1) / 50.
*H21
      B(H11NODE(4),1) = (B(H11NODE(3),1) - B(H11NODE(4),1))
     */ HVALUE(2)
      B(H11NODE(4),2) = (B(H11NODE(3),2) - B(H11NODE(4),2))
     */ HVALUE(2)
      CALL    DIVI(B(H11NODE(4),1),B(H11NODE(4),2),
     *B(H11NODE(2),1),B(H11NODE(2),2),C1,C2)
      CH(3) = CMPLX (C1,C2)
      H21 = CH(3)
         HM = CABS(H21)
         HP = 180.*2.*ATAN((HM-REAL(H21))/AIMAG(H21)) / PI
         WRITE (12,*) FREQ,HM,HP
      ELSE
*H12
      CALL DIVI(B(H22NODE(1),1),B(H22NODE(1),2),
     *B(H22NODE(3),1),B(H22NODE(3),2),C1,C2)
      CH(2) = CMPLX (C1,C2)
      H12 = CH(2)
         HM = CABS(H12)
         HP = 180.*2.*ATAN((HM-REAL(H12))/AIMAG(H12)) / PI
         WRITE (13,*) FREQ,HM,HP
*H22
      B(H22NODE(4),1) = (B(H22NODE(3),1) - B(H22NODE(4),1))
     */ HVALUE(4)
      B(H22NODE(4),2) = (B(H22NODE(3),2) - B(H22NODE(4),2))
     */ HVALUE(4)
      CALL DIVI(B(H22NODE(4),1),B(H22NODE(4),2),
     *B(H22NODE(3),1),B(H22NODE(3),2),C1,C2)
      CH(4) = CMPLX (C1,C2)
      H22 = CH(4)
         HM = CABS(H22)
         HP = 180.*2.*ATAN((HM-REAL(H22))/AIMAG(H22)) / PI
         WRITE (14,*) FREQ,HM,HP
```

```
      CH(4) = CH(4) * 50.
      END IF
CCC   CLEAR A( ),B( ),WA( )  CCC
      DO 71 III = 1,NMAX(I)
         B(III,1) = 0.0
         B(III,2) = 0.0
      DO 71 JJJ = 1,NMAX(I)
         A(III,JJJ,1) = 0.0
         A(III,JJJ,2) = 0.0
71    CONTINUE
50    CONTINUE
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C                                                                      C
C        CALCULATE Y-PARAMETERS                                        C
C                                                                      C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
      Y11=1./H11
      Y21=H21/H11
      Y12=-H12/H11
      Y22=H11*H22-H12*H21
      Y22=Y22/H11
* Y11
        YY = AIMAG(Y11)/W
         YM = CABS(Y11)
         YP = 180.*2.*ATAN((YM-REAL(Y11))/AIMAG(Y11)) / PI
         WRITE (15,*) FREQ,YM,YP
*Y21
        YY = AIMAG(Y21)/W
         YM = CABS(Y21)
         YP = 180.*2.*ATAN((YM-REAL(Y21))/AIMAG(Y21)) / PI
         WRITE (16,*) FREQ,YM,YP
*Y12
        YY = AIMAG(Y12)/W
         YM = CABS(Y12)
         YP = 180.*2.*ATAN((YM-REAL(Y12))/AIMAG(Y12)) / PI
         WRITE (17,*) FREQ,YM,YP
*Y22
        YY = AIMAG(Y22)/W
         YM = CABS(Y22)
         YP = 180.*2.*ATAN((YM-REAL(Y22))/AIMAG(Y22)) / PI
         WRITE (18,*) FREQ,YM,YP
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C                                                                      C
C        CALCULATE S-PARAMETERS                                        C
C                                                                      C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
      CSN  =  (CH(1) + 1.) * (CH(4) + 1.) - CH(2) * CH(3)
      CS11 = ((CH(1) - 1.) * (CH(4) + 1.) - CH(2) * CH(3)) /
```

```
     *       CSN
      CS12 =  2. * CH(2) / CSN
      CS21 = -2. * CH(3) / CSN
      CS22 = ((CH(1) + 1.) * (-CH(4) + 1.) + CH(2) * CH(3)) /
     *       CSN
          SM = CABS(CS11)
          SP = 180.*2.*ATAN((SM-REAL(CS11))/AIMAG(CS11)) / PI
          WRITE (19,*) FREQ,SM,SP
          SM = CABS(CS21)
          SP = 180.*2.*ATAN((SM-REAL(CS21))/AIMAG(CS21)) / PI
          WRITE (20,*) FREQ,SM,SP
          SM = CABS(CS12)
          SP = 180.*2.*ATAN((SM-REAL(CS12))/AIMAG(CS12)) / PI
          WRITE (21,*) FREQ,SM,SP
          SM = CABS(CS22)
          SP = 180.*2.*ATAN((SM-REAL(CS22))/AIMAG(CS22)) / PI
          WRITE (22,*) FREQ,SM,SP
111   CONTINUE
      DO 80 I = 11,22
           CLOSE (UNIT = I, STATUS = 'KEEP')
80    CONTINUE
210   FORMAT (A3,BN,2(1X,I2),1X,BN,G10.1)
220   FORMAT (3X,BN,4(1X,I2),BN,2(1X,G10.1))
      STOP
      END
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C                                                                      C
C       SUBROUTINE: GAUSS-ELIMINATION                                  C
C                                                                      C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
      SUBROUTINE GE(N)
      IMPLICIT REAL*12 (A-B)
      INTRINSIC QABS,QSQRT
      INTEGER N,T,NROW(30),MAXN
      REAL*12 S(30,2)
      REAL*12 MAX,TEMP,C1,C2,SUM1,SUM2
      COMMON /CC/ A(20,20,2),B(20,2)
      DO 300 T = 1,N
      A(T,(N+1),1) = B(T,1)
      A(T,(N+1),2) = B(T,2)
300   CONTINUE
CCC INITIALIZE ROW POINTER CCC
      DO 301 II = 1,N
         NROW(II) = II
         MAX = 0.
         DO 302 JJ = 1,N
            DO 302 KK = 1,2
               TEMP = QABS(A(II,JJ,KK))
```

```
               IF (TEMP .GT. MAX) THEN
               MAXN = JJ
               MAX = TEMP
               END IF
302         CONTINUE
         IF (MAX .EQ. 0.) THEN
            WRITE (6,*) 'NO UNIQUE SOLUTION EXISTS'
            STOP
         END IF
         S(II,1) = A(II,MAXN,1)
         S(II,2) = A(II,MAXN,2)
301   CONTINUE
CCC SCALING EACH ROW WITH S( , ) CCC
      DO 400 II = 1,N
         DO 400 JJ = 1,N+1
         A1 = A(II,JJ,1)
         A2 = A(II,JJ,2)
         B1 = S(II,1)
         B2 = S(II,2)
         CALL DIVI(A1,A2,B1,B2,C1,C2)
         A(II,JJ,1) = C1
         A(II,JJ,2) = C2
400   CONTINUE
CCC MAIN LOOP (ELIMINATION PROCESS) CCC
      DO 410 II = 1,(N-1)
        MAX = 0.
         DO 420 JJ = II,N
            TEMP = A(JJ,II,1)*A(JJ,II,1) +
     *             A(JJ,II,2)*A(JJ,II,2)
            TEMP = QSQRT(TEMP)
            IF (TEMP .GT. MAX) THEN
            NTEMP = JJ
            MAX = TEMP
            END IF
420      CONTINUE
         IF (MAX .EQ. 0.) THEN
            WRITE (6,*) 'NO UNIQUE SOLUTION EXISTS'
            STOP
         END IF
         IF (NROW(II) .NE. NTEMP) THEN
            NCOPY = NROW(II)
            NROW(II) = NTEMP
            NROW(NTEMP) = NCOPY
         END IF
         DO 440 JJ = (II+1),N
            A1 = A(NROW(JJ),II,1)
            A2 = A(NROW(JJ),II,2)
            B1 = A(NROW(II),II,1)
```

```
            B2 = A(NROW(II),II,2)
            CALL DIVI(A1,A2,B1,B2,C1,C2)
            DO 440 KK = 1,(N+1)
               A(NROW(JJ),KK,1) = A(NROW(JJ),KK,1)
     * - C1*A(NROW(II),KK,1) + C2*A(NROW(II),KK,2)
               A(NROW(JJ),KK,2) = A(NROW(JJ),KK,2)
     * - C1*A(NROW(II),KK,2) - C2*A(NROW(II),KK,1)
440         CONTINUE
410         CONTINUE
      IF(A(NROW(N),N,1).EQ.0..AND.A(NROW(N),N,2).EQ.0.) THEN
            WRITE (6,*) 'NO UNIQUE SOLUTION EXISTS'
            STOP
      END IF
CCC START BACKWARD SUBSTITUTION CCC
      A1 = A(NROW(N),N+1,1)
      A2 = A(NROW(N),N+1,2)
      B1 = A(NROW(N),N,1)
      B2 = A(NROW(N),N,2)
      CALL DIVI(A1,A2,B1,B2,C1,C2)
      B(N,1) = C1
      B(N,2) = C2
      DO 500 II = (N-1),1,-1
        SUM1 = 0.
        SUM2 = 0.
         DO 510 LL = (II+1),N
            SUM1 = SUM1 + A(NROW(II),LL,1)*B(LL,1)
     *                  - A(NROW(II),LL,2)*B(LL,2)
            SUM2 = SUM2 + A(NROW(II),LL,1)*B(LL,2)
     *                  + A(NROW(II),LL,2)*B(LL,1)
510      CONTINUE
         SUM1 = A(NROW(II),(N+1),1) - SUM1
         SUM2 = A(NROW(II),(N+1),2) - SUM2
         B1 = A(NROW(II),II,1)
         B2 = A(NROW(II),II,2)
         CALL DIVI(SUM1,SUM2,B1,B2,C1,C2)
         B(II,1) = C1
         B(II,2) = C2
500   CONTINUE
      RETURN
      END
      SUBROUTINE DIVI(A1,A2,B1,B2,C1,C2)
      REAL*12 A1,A2,B1,B2,C1,C2,Z
      C1 = B1*A1 + B2*A2
      C2 = B1*A2 - B2*A1
      Z = B1*B1 + B2*B2
      C1 = C1 /Z
      C2 = C2 /Z
      RETURN
```

```
END
SUBROUTINE MULTI(A1,A2,B1,B2,C1,C2)
REAL*12 A1,A2,B1,B2,C1,C2
C1 = A1*B1 - A2*B2
C2 = A1*B2 + A2*B1
RETURN
END
```

APPENIDIX C
S-PARAMETER MEASUREMENT CALIBRATION

The two-port small-signal network can be analyzed in terms of H-, Y-, or z-parameters [HEWL72]. Therefore, to analyze the frequency response of high-speed BJT, we need to measure these small-signal output parameters. All of these parameters relate total voltages and total currents at each port. Measuring these parameters calls for the input and output of the network to be successively open and short circuited. However, at high-frequencies (over 100 MHz) it is very difficult to achieve short and open circuits over a broad band of frequency. To overcome this problem, s-parameters are usually measured, because in measuring s-parameters, open- and short-circuits are not used. Instead, the load impedance which is the characteristic impedance (50 ohm) is used to prevent the reflection from the load. The scattering parameters (s-parameters) are defined in terms of traveling waves instead of voltages and currents. For example, the relations between s-parameters and h-parameters are derived through square roots of incident and reflected powers from the two ports. Therefore, the measured s-

parameters can be transformed into any of H-, Z-, or y-parameters using related formula.

s-parameters is measured using HP8510 Automated Network Analyzer which can measure up to 26.5 GHZ and HP4145A Semiconductor Parameter Analyzer as a DC power supply source. Although the network analyzer can measure s-parameters up to very high frequency, the calibration technique and the quality of coaxial cable and probes can limit its capability. Recent developments in high frequency measurement instrumentation have greatly improved the characterization of high-speed transistors. In particular, the possibility of "On wafer" s-parameter measurements at frequencies up to 20 GHz with the Cascade Microtech probes can be a great achievement.

However, for the advanced small-size transistor, not only accurate instrumentation, but also an accurate calibration of the device under test (DUT) from its environment, i.e. parasitics. These parasitics include the effects of bonding pads, device connection metal lines, and substrate resistance, which have a dramatic impact on the measured s-parameter of a DUT. Therefore, the accurate and reliable calibration procedure is needed.

The important thing with calibrating a measurement system is to define a certain reference plane and improve accuracy. The calibration procedure used for this work is

based on the full two-port error model which is implemented in the HP 8510 and TECAP software. It is based on a twelve error-term model, directivity, source match, load match, reflection frequency response, transmission frequency response and isolation, for forward and reverse and therefore requires 12 measurements.

There are three calibration techniques [FRAS88] available for on-silicon-wafer s-parameter measurement. They are as follows:

(1) ISS (impedance standard substrate) calibration

The procedure is to calibrate the network analyzer and wafer probe system at the probe tips using an open, short, load, and through on the well-understood ISS. On wafer measurement after this calibration method includes the parasitics of pads and interconnect metal lines in the measurement. As a result, Device performance can be underestimated.

(2) ISS calibration and subtract y-parameters

The first procedure is to calibrate system using ISS on glass as above procedure (1). This procedure establishes a reference plane at the tip of the probes. Then measure the open pattern which includes contact pads, interconnect metal line without DUT. Now, s-parameters of a DUT embedded in open pattern (Dummy) are measured. In many cases all the important

parasitics are in parallel with DUT and can be modeled with resistors, capacitors, and inductors (see Fig.6.2). By transforming the s-parameters to y-parameters for both Device with Dummy and Dummy, correct for the environment in the y-parameter domain using the following relation (see Fig. C.1).

Measured Dummy y-parameters

$$Y_{11d} = G_{d1} + G_{d2} \quad (C.1)$$

$$Y_{12d} = - G_{d2} \quad (C.2)$$

$$Y_{21d} = - G_{d2} \quad (C.3)$$

$$Y_{22d} = G_{d2} + G_{d3} \quad (C.4)$$

Measured DUT (with Dummy) y-parameters

$$Y_{11m} = G_{d1} + G_{d2} + Y_{11t} \quad (C.5)$$

$$Y_{12m} = - (G_{d2} + Y_{12t}) \quad (C.6)$$

$$Y_{21m} = - (G_{d2} + Y_{21t}) \quad (C.7)$$

$$Y_{22m} = G_{d2} + G_{d3} + Y_{22t} \quad (C.8)$$

Corrected DUT y-parameters

$$Y_{11m} = Y_{11m} - Y_{11d} \quad (C.9)$$

$$Y_{12m} = Y_{12m} - Y_{12d} \quad (C.10)$$

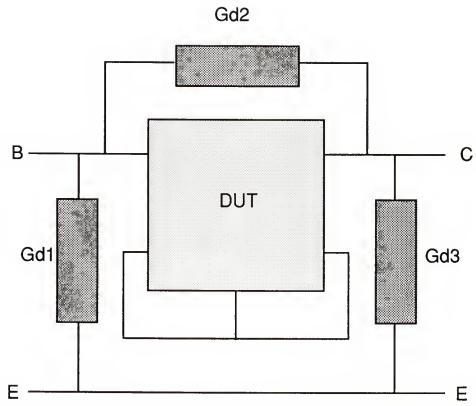


Fig. C.1 Representation of the parasitic admittance branches in parallel with the DUT.

$$Y_{21m} = Y_{21m} - Y_{21d} \quad (C.11)$$

$$Y_{22m} = Y_{22m} - Y_{22d} \quad (C.12)$$

In this method, the layout of the open pattern is the most critical. The DUT metallization pattern and the open pattern standard should match, so that the interconnect parasitics can be accounted for.

(3) Silicon calibration

The procedure is to calibrate the network analyzer and wafer probes using on-wafer calibration standards, which should be included along with the DUT. Besides open pattern, the other calibration pattern to consider is the load, which ideally should be 50 ohms. Most silicon processes do not provide precision resistors. This can be accounted for in two ways: (1) measure the actual value of the load resistor and enter that value in the HP 8510 and (2) create several loads of slightly different values so that one of them will be acceptably close to 50 ohms.

The cut-off frequencies and s-parameters measured using the above methods result in differences in frequency of 5 to 6 GHz. The first method underestimates f_t because it does not subtract out the effects of the pads. The third method may overestimate f_t compared to the second method, which yielding intermediate results is the most reasonable calibration

technique [FRAS88]. However, if the on-wafer calibration standard were made ideally, the result of the second method should have been the same as the third method.

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